Total No. of Questions : 10]

SEAT No. :

**P2246**

[Total No. of Pages : 3

# [5254]-581
## B.E. (Electronics) (Semester -I)
## VLSI DESIGN
## (2012 Pattern)

*Time : 2.30 Hours]* *[Max. Marks : 70*

***Instructions to the candidates:***

1) ***Attempt Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8, Q9 or Q10.***

2) ***Draw neat diagrams.***

3) ***Assume Suitable data if necessary.***

***Q1)*** a) What is power delay product? Derive the expression for it. What is its significance? **[6]**

b) Explain Body effect and Channel length modulation in detail. **[4]**

OR

***Q2)*** a) What is VHDL code to infer following RTL shown in fig 1. What do you mean by FDC? **[6]**

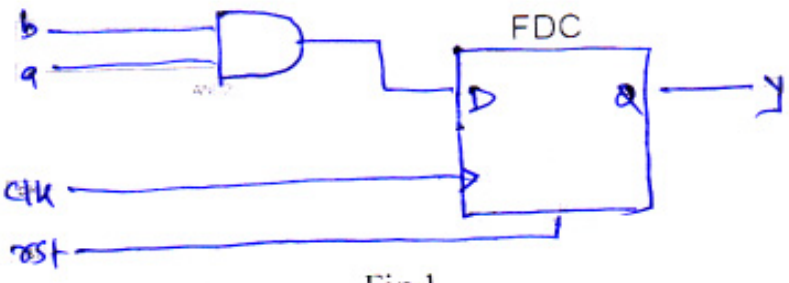


Fig 1

b) What are packages with an example. **[4]**

***P.T.O***

***Q3)*** a) Explain CPLD architecture in detail. What do you understand by xc9572-7pc84 number? **[6]**

b) Draw CMOS inverter circuit and explain voltage transfer characteristics. **[4]**

OR

***Q4)*** a) How logic is implemented in FPGA? Explain with half adder circuit configuration. **[6]**

b) Compare PROM, PLA, PAL and CPLD. **[4]**

***Q5)*** a) Compare SRAM and DRAM. **[8]**

b) What is the role of memories in PLDs? Explain in detail. **[8]**

OR

***Q6)*** a) Which different refresh circuits are available for memories? Explain detail. **[8]**

b) Explain working of DRAM in detail. Why it is preferred though it is slower? **[8]**

***Q7)*** a) Explain switch box routing with its advantages. **[8]**

b) What assumptions are made in estimating path delays? Which router is used to remove same assumptions? **[8]**

OR

***Q8)*** a) What are goals and objectives of detail routing. **[8]**

b) What is important difference between path and net when Global router minimizes delay? **[8]**

***Q9)*** a) Explain TAP Controller in detail. **[9]**

b) Explain controllability measure with an example. **[9]**

OR

***Q10)***a) What is need of Design for testability? **[9]**

b) What is partial scan and full scan checks? **[9]**

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