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Seat No.	
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[5057]-2050

S.E. E&TC (Electronics) (First Semester) EXAMINATION, 2016

DIGITAL ELECTRONICS

(2015 PATTERN)

Time : Two Hours

Maximum Marks : 50

N.B. :— (i) Answer Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4,
Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Use of calculator is allowed.

(v) Assume suitable data, if necessary.

1. (a) Design of one bit magnitude comparator. [4]
- (b) Convert SR flip-flop to Toggle flip-flop (SR to TFF). [4]
- (c) Compare the multiplexer and de-multiplexer. [4]

Or

2. (a) Implement the following expression using single 8 : 1 multiplexer : [6]
$$Y = \sum m (0, 1, 2, 5, 7, 8, 9, 14, 15)$$
- (b) What are advantages of master-slave JK flip-flop ? Explain the working with a suitable diagram. [6]

P.T.O.

3. (a) Design a sequence generator for the sequence ..10110... [6]
(b) Compare TTL and CMOS logic family with reference to the following characteristics : [6]
- (i) fanout
 - (ii) propagation delay
 - (iii) Power dissipation
 - (iv) noise margin
 - (v) speed power product
 - (vi) voltage and current parameters.

Or

4. (a) Explain the terms related to ASM chart : [6]
- (i) state box
 - (ii) decision box
 - (iii) conditional box
- (b) Draw and explain working of two input TTL NAND gate and list advantages of totem pole output stage. [6]

5. (a) A combinational circuit is defined by functions : [6]

$$F1 = \sum m (3, 5, 7)$$

$$F2 = \sum m (4, 5, 7)$$

Design the circuit using PLA having 3 inputs, 3 product terms and 2 outputs.

- (b) Draw circuits of one cell of dynamic RAM and explain its working. [4]
- (c) Compare SRAM and DRAM. [3]

Or

- 6. (a) Draw and explain the internal organization of asynchronous SRAM. [6]
- (b) Explain PLA with the help of neat diagram. [4]
- (c) Compare CPLD and FPGA. [3]

- 7. (a) Draw and explain architecture of 8051 in detail. [6]
- (b) Compare the microprocessor and microcontroller. [4]
- (c) Write a program for addition of 8-bit binary numbers. [3]

Or

- 8. (a) Explain any *three* addressing modes of 8051 with example. [6]
- (b) Draw and explain PSW register of 8051. [4]
- (c) List out features of 8051 (minimum *six*). [3]