Scheme – I
Sample Question Paper

Program Name : **Electronics and Telecommuication Engineering Group**

Program Code : **DE,IE.**

22639

Semester : **SIXTH**

Course Title : **Very Large Scale Integration(VLSI)**

Marks : **70** **Time:3Hrs.**

Instructions:

(1) All questions are compulsory.

(2) Illustrate your answers with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data if necessary.

(5) Preferably, write the answers in sequential order.

Q.1) Attempt any FIVE of the following :- **(10 Marks)**

(a) Define the terms: Metastability and Noise margin.

(b) Write two examples of concurrent construct in VHDL.

(c) List the data types in VHDL.

(d) Write the applications of test bench.

(e) Define Moore machine and draw the diagram for it.

(f) State the concept of Zero Modeling.

(g) Draw the schematic diagram of transmission gate and write the advantage of it.

Q.2) Attempt any THREE of the following :- **(12 Marks)**

(a) Explain with block diagram the architecture of CPLD.

(b) Write the VHDL code for 3 bit up counter using sequential construct.

(c) Draw the circuit of CMOS inverter and its characteristic.

(d) Explain the HDL design flow for synthesis process.

Q.3) Attempt any THREE of the following. **(12 Marks)**

(a) Explain the estimation process of resistance with layout diagram.

(b) Write the VHDL code for 4:1 Multiplexer.

(c) Explain various data types used in VHDL.

(d) Write the Pro's and Con's of VHDL.

Q.4) Attempt any THREE of the following. (12 Marks)

(a) Compare CPLD and FPGA on the basis of flexibility , capacity and any other two parameters.

(b) Design following function using CMOS logic—

$F = \overline{([A+B]\ \overline{[C+D]})}$

(c) Explain the different delays in VHDL simulation.

(d) Draw the CMOS transistor cross-section diagram and layout diagram using Twin tub process

(e) Explain the following terms with respective VHDL with example--

i. Entity , ii. Architecture.

Q.5) Attempt any TWO of the following. (12 Marks)

(a) Design the Moore or Mealy machine for detecting the sequence 1101.

(b) Explain any two processes – i) Oxidation, ii) Ion implantation, iii) Gate fabrication.

(c) Write the VHDL code for 2 input Ex-OR gate using –

i) Behavioural modeling and ii) Data flow modeling.

Q.6) Attempt any TWO of the following. (12 Marks)

a) Explain the VLSI design flow with neat sketch.

b) Explain ASIC design flow with neat sketch.

c) Write the syntax and use of any two – i) signal, ii) variable, iii) constant.

Scheme – I
Sample Test Paper - I

Program Name : **Electronics and Telecommunication Engineering Group**

Program Code : **DE,IE**

22639

Semester : **SIXTH**

Course Title : **Very Large Scale Integration**

Marks : **20** **Time:1 Hour**

Instructions:

(1) All questions are compulsory.

(2) Illustrate your answers with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data if necessary.

(5) Preferably, write the answers in sequential order.

Q.1 Attempt any FOUR. **(08 Marks)**

a) Define the terms: Skew and Fan-out.
b) Write one example of concurrent and sequential construct in VHDL.
c) List various data types in VHDL.
d) Write the name of the test bench tool and HDL entry tool.
e) Write the meaning of part number of Xilinx FPGA IC XC4VLX60-10FFG668CS2. (any two).
f) Define FSM and write the output of Mealy machine.

Q.2 Attempt any THREE. **(12 Marks)**

(a) Explain FPGA architecture with block diagram.
(b) Write the VHDL code for 3 bit down counter.
(c) Write the Con's of VHDL.
(d) Using Behavioral modeling, write the code for AND gate.

Scheme – I
Sample Test Paper - II

Program Name : **Electronics and Telecommunication Engineering Group**

Program Code : **DE,IE.**

22639

Semester : **SIXTH**

Course Title : **Very Large Scale Integration**

Marks : **20** **Time:1 Hour**

Instructions:

(1) All questions are compulsory.

(2) Illustrate your answers with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data if necessary.

(5) Preferably, write the answers in sequential order.

Q.1 Attempt any FOUR. **(08 Marks)**

(a) State the use of sensitivity list using the syntax for it.
(b) Define HDL simulation.
(c) State the effective coding styles in VHDL.
(d) Draw circuit of 2 input NAND gate using with CMOS logic.
(e) State advantages of Twin Tub.

Q.2 Attempt any THREE. **(12Marks) (3X4)**

a) Explain event scheduling in VHDL.
b) Compare between software and hardware description language
c) Compare the performance parameters of BJT and CMOS logic family.
d) Design following function using CMOS logic—

$$F = \overline{([AB] + [CD])}$$