Scheme – I

Sample Question Paper

Program Name : **Diploma in Digital Electronics**
Program Code : **DE**
Semester : **Fifth**
Course Title : **Digital System Applications**
Marks : **70** **Time: 3 Hrs.**

22536

Instructions:

(1) All questions are compulsory.
(2) Illustrate your answers with neat sketches wherever necessary.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary.
(5) Preferably, write the answers in sequential order.

Q.1 Attempt any FIVE of the following. **10 Marks**

a) Draw a 4 bit even parity generator circuit using X-OR gate.
b) Differentiate between combinational logic circuit and sequential logic circuit.
c) Draw the state transition diagram for sequence '110' by using Mealy machine.
d) Define hazards. List its types.
e) Differentiate between synchronous sequential circuit and asynchronous sequential circuit.
f) State any two advantages of PLAs.
g) Draw single decimal digit common anode type display using 7447 decoder and decade counter.

Q.2 Attempt any THREE of the following. **12 Marks**

a) Use Q-M approach to minimize the function:
F (A, B, C, D, E) = $\sum$ m (0, 1, 2, 7, 9, 11, 12, 23, 27, 28)
b) Design a 16-to-1 multiplexer using two 8-to-1 multiplexers having an active low ENABLE input.
c) Draw the state transition diagram of two bit up counter.
d) Draw and describe the block diagram of asynchronous sequential circuit with neat sketch.

Q.3 Attempt any THREE of the following. **12 Marks**

a) Design a full subtractor using 3-to-8 decoder and logic gates.

b) Describe the state reduction method (any one) to design synchronous sequential circuit.

c) Describe the race condition in asynchronous sequential circuit. Also state method to avoid races.

d) Draw the internal architecture of PLA device and describe it.

Q.4 Attempt any THREE of the following. **12 Marks**

a) Design J K flip flop using T flip flop.

b) Design S R flip flop using D flip flop.

c) Design a full adder using PLA.

d) Describe CPLD with its architecture.

e) Describe with neat diagram basic instrument to measure time period.

Q.5 Attempt any two of the following. **12 Marks**

a) Design a sequence generator for sequence 011 using Moore model and implement using D flip flop.

b) Design a PLA device to implement a magnitude comparator to produce outputs for A_1 A_0 being equal to**,** not equal to, less than and greater than B_1B_0.

c) Describe the instrument to measure time with block diagram. Consider unknown input is 200 Hz square wave.

Q.6 Attempt any two of the following. **12 Marks**

a) Implement the following Boolean functions with PLA:

$F_1 (A, B, C) = \sum (0, 1, 2, 4)$

$F_2 (A, B, C) = \sum (0, 5, 6, 7)$

b) Design and draw common anode type single decimal digit display for clock frequency 1 Hz using 7-segment decoder IC 7448 and decade counter.

c) Design a 4 digit frequency counter using 54/74143 and 54/74160. Use a 1.0 MHz clock and provide 0.1 sec, 1.0 sec and 10 sec gate.

Scheme – I

Sample Test Paper - I

Program Name : **Diploma in Digital Electronics**
Program Code : **DE**
Semester : **Fifth**
Course Title : **Digital System Applications**
Marks : **20**

22536

Time: 1 Hour.

Instructions:

(1) All questions are compulsory.
(2) Illustrate your answers with neat sketches wherever necessary.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary.
(5) Preferably, write the answers in sequential order.

Q.1 Attempt any FOUR. **08 Marks**

a) Define decoder. Draw logic diagram for 2-to-4 line decoder.

b) Draw a state transition diagram of sequence detector circuit that detects '1101' from input
data stream using Mealy model.

c) Obtain the state synthesis table for the given (figure 1) state transition diagram of Moore
model.

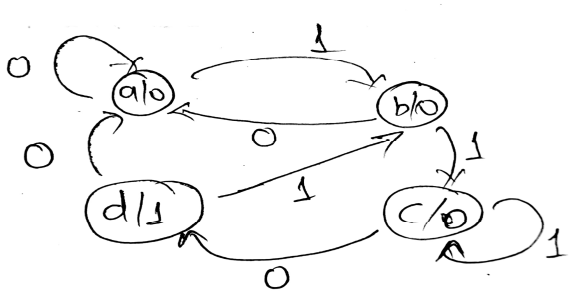

Figure 1

d) Define static 0 and static 1 hazard.

e) Define race condition in digital circuits with suitable example.

f) Describe dynamic hazard and its elimination.

Q.2 Attempt any THREE. **12 Marks**

a) Design a comparator that will compare the two words A = $(A_1A_0)_2$ and B = $(B_1B_0)_2$ in binary code.

b) Reduce the state transition diagram of given figure 2 by Row elimination method or Implication table method.

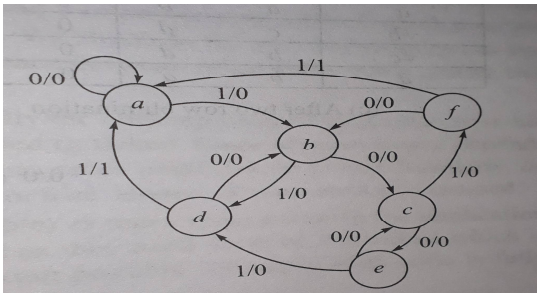

Figure 2

c) Construct an ASM chart for 2 bit up counter.

d) State the steps to design asynchronous sequential circuit.

e) Design SR flip flop using JK flip flop.

Scheme – I

Sample Test Paper - II

Program Name : **Diploma in Digital Electronics**
Program Code : **DE**
Semester : **Fifth**
Course Title : **Digital System Applications**
Marks : **20**

22536

Time: 1 Hour

Instructions:

(1) All questions are compulsory.

(2) Illustrate your answers with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data if necessary.

(5) Preferably, write the answers in sequential order.

Q.1 Attempt any FOUR. **08 Marks**

a) State the applications of PLA.

b) State the difference between PAL and GAL.

c) Find the value displayed by basic frequency counter if unknown input signal is 7.5 KHz square wave and gate enable time is t = 0.1 sec.

d) Draw digit control waveform of four digit multiplexed display.

e) Draw the block diagram of instrument to measure time.

f) Draw the pin diagram of ADD 3501.

Q.2 Attempt any THREE. **12 Marks**

a) Compare CPLD and FPGA (any 4 points).

b) Design the following combinational logic circuit using PLA

$Y_1 = \sum m (0, 3, 5, 6, 9, 10, 12, 15)$

$Y_2 = \sum m (0, 1, 2, 11, 14, 15)$

c) Design and draw common cathode type single decimal digit display for clock frequency 1 Hz using 7-segment decoder IC 7447 and decade counter.

d) Describe basic frequency counter with neat block diagram.

e) Describe four decimal digits, period measurement instrument with neat block diagram.