SUMMER – 2022 EXAMINATION

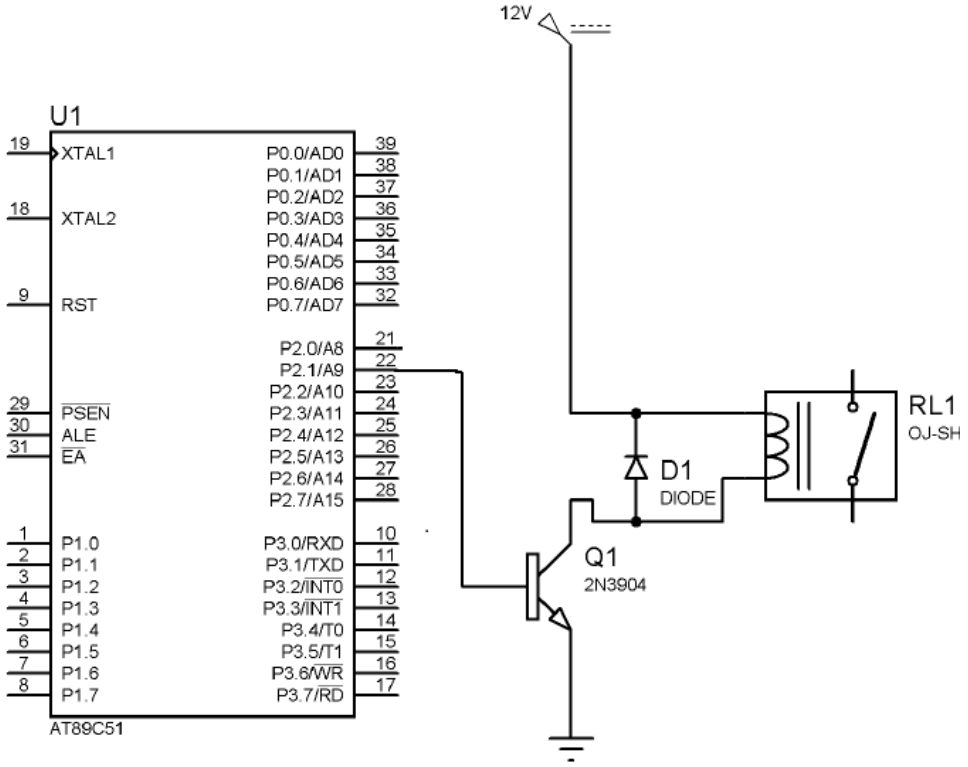
Subject Name: Microcontroller and Application **Model Answer** **Subject Code:** **22426**

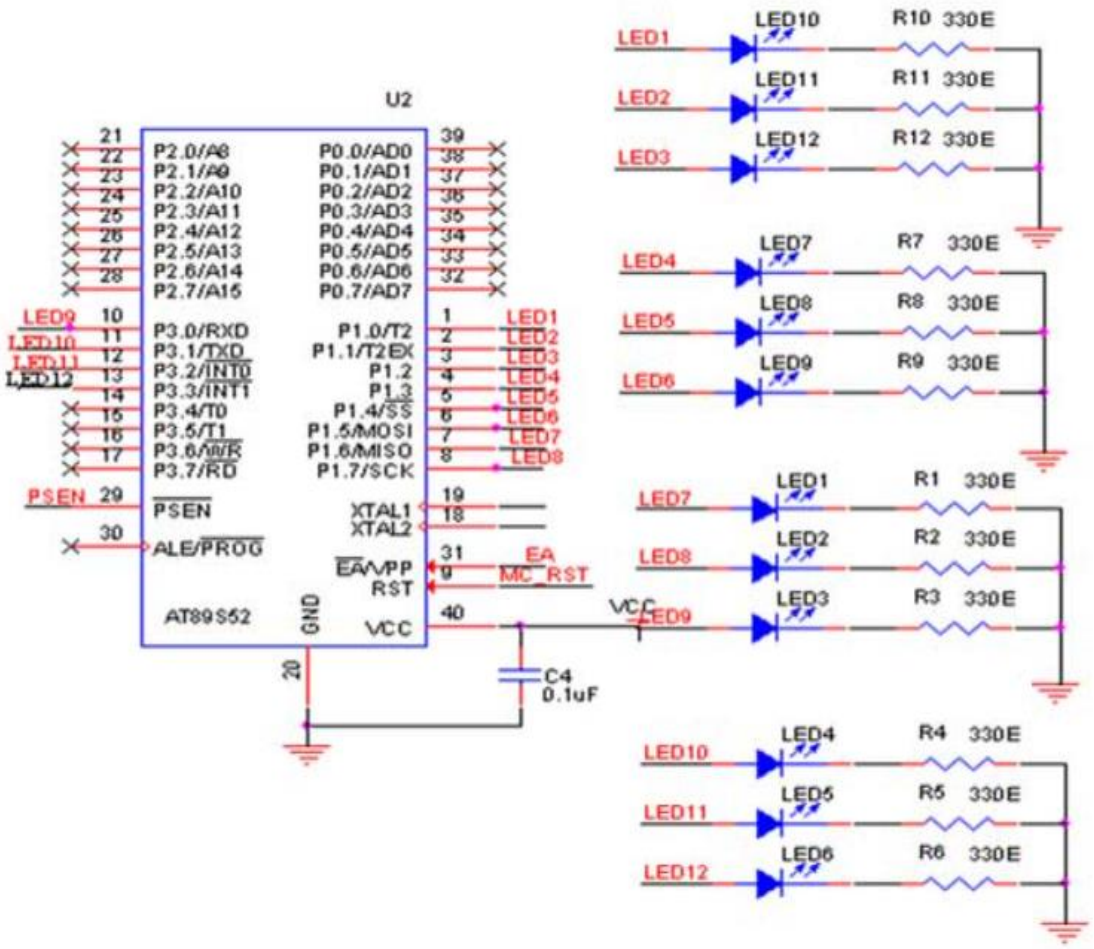
Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.
8) As per the policy decision of Maharashtra State Government, teaching in English/Marathi and Bilingual (English + Marathi) medium is introduced at first year of AICTE diploma Programme from academic year 2021-2022. Hence if the students in first year (first and second semesters) write answers in Marathi or bilingual language (English +Marathi), the Examiner shall consider the same and assess the answer based on matching of concepts with model answer.

Q. No.	Sub Q.N.	Answer	Marking Scheme
Q.1		**Attempt any FIVE of the following :**	**10-Total Marks**
	a)	**State function of PSEN and EA pins of 8051 microcontroller.**	**2M**
	Ans:	**PSEN:** This is an output pin. PSEN stands for "program store enable." It is active low O/P signal. It is used to enable external program memory (ROM). When [PSEN(bar)]= 0, then external program memory becomes enabled and micro controller read content of external memory location. Therefore it is connected to (OE) of external ROM. **EA:** It is an active low I/P to 8051 microcontroller. EA stands for "External Access". When (EA) = 0, then 8051 microcontroller access from external program memory (ROM) only. When (EA) = 1, then it access internal and external program memories (ROMS).	**1M** **1M**
	b)	**State maximum size of external memory that can be interfaced with 8051 mc. Explain it.**	**2M**

	Ans:	A maximum of 64 KB of external memory can be interfaced with 8051 microcontroller. **Explanation:** As 8051microcontroller is having 16-bit address bus, it can access 2^16 memory locations. 64KB (65536) each of RAM and ROM.	1M 1M
	c)	**Define stack. Write size of stack pointer.**	2M
	Ans:	**Stack:** The stack is a section of a RAM used by the CPU to store information such as data or memory address on temporary basis. **Size of stack pointer:** 8 bit	1M 1M
	d)	**Draw format of IE and IP SFRS.**	2M
	Ans:	**Format of IE SFR:** IE.7 IE.6 IE.5 IE.4 IE.3 IE.2 IE.1 IE.0 EA -- -- ES ET1 EX1 ET0 EX0 **Format of IP SFR:** IP.7 IP.6 IP.5 IP.4 IP.3 IP.2 IP.1 IP.0 -- -- PT2 PS PT1 PX1 PT0 PX0	1M 1M
	e)	**Define the term bus. Write size of buses in 8051 µc.**	2M
	Ans:	**BUS:** A Bus is a set of physical connections used for communication between CPU and peripherals. Different buses used in microcontroller are: **1. Address Bus:** 16 bit **2. Data Bus:** 8 bit **3. Control Bus:** 1 bit	1M 1M
	f)	**Draw interfacing diagram of relay connected to 2.1 of 8051 µc.**	2M

	Ans:	**Interfacing diagram:** 	**2M (Clock circuit and Reset circuit can also be additionally drawn)**
	g)	**Give different applications of stepper motor.**	**2M**
	Ans:	**Applications of stepper motor.** 1. floppy disk drives, 2. flatbed scanners, 3. computer printers, 4. plotters, 5. Small robotics. 6. slot machines, 7. image scanners, 8. compact disc drives, 9. intelligent lighting, 10. camera lenses, 11. CNC machines, 12. 3D printers.	**Any 4** **½ M each**

Q.2		Attempt any THREE of the following :	12- Total Marks
	a)	**Draw a interfacing diagram of traffic light controller with 8051.**	4M
	Ans:	**Interfacing Diagram of traffic light controller with 8051:** 	4M

b) Compare Microprocessor and Microcontroller. **4M**

Ans:

Sr.No.	Parameter	Microprocessor	Microcontroller
1	No. of instruction used	Many instruction to read write data to/from external memory.	Few instruction to read/write data to/from external memory.
2	Memory	Do not have inbuilt RAM or ROM	Inbuilt RAM/ROM
3	Registers	Microprocessor contains general purpose registers,stack pointer register program counter register	Microcontroller contains general purpose registers,stack pointer register program counter register additional to that it contains Special Function registers(SFRs) for timer Interrupt and serial communication etc.
4	Timer	Do not have inbuilt timer	Inbuilt timer
5	I/O Ports	I/O ports not available requires extra device like 8155 or 8255	I/O ports are available
6	Serial Port	Do not have inbuilt serial port requires extra device like 8155 or 8255.	Inbuilt serial port
7	Multifunction pins	Less multifunction pins on IC	any multifunction pins on the IC
8	Boolean Operation	Boolean Operation is not possible directly	Boolean Operation i.e Operation on individual but is possible directly.
9	Applications	General purpose Computers and personal uses	Single Purpose (dedicated application) , Automobile companies embedded systems remote control devices.

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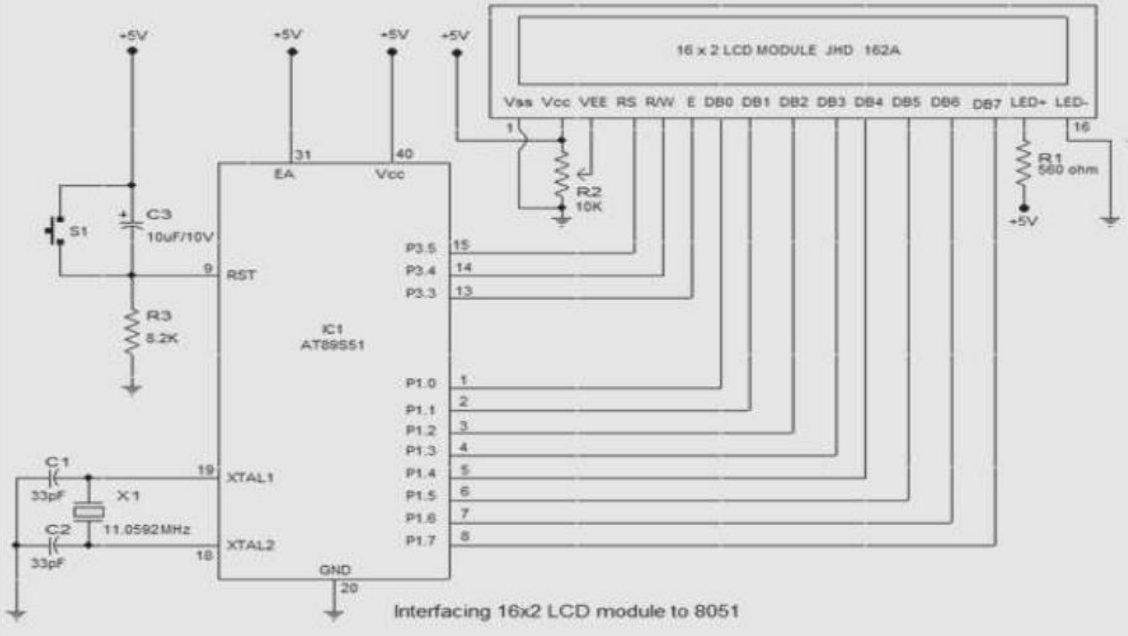
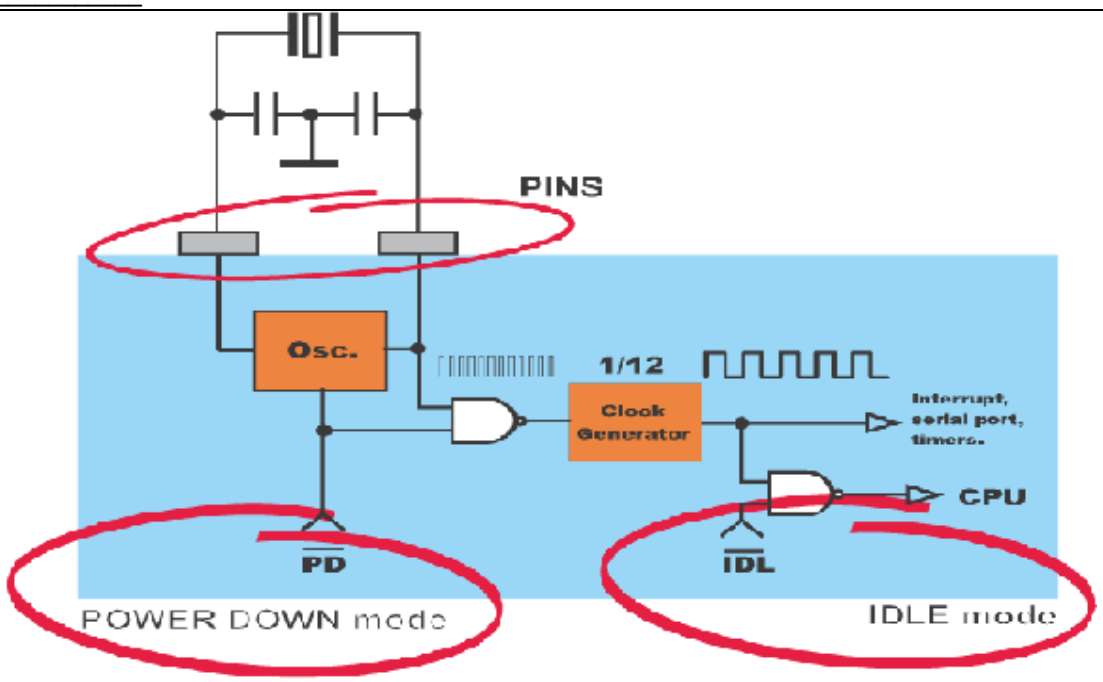
Any 4 points

Each point 1M

	c)	**Draw format of PCON SFR. State use of SMOD bit.**	**4M**
	Ans:	**Format of PCON SFR:** PCON: POWER CONTROL REGISTER.NOT BIT ADDRESSABLE. **SMOD** | **——-** | **—–** | **——** | **GF1** | **GF0** | **PD** | **IDL** **S**MOD Double baud rate bit.If Timer 1 is used to generate baud rate and SMOD=1, the baud rate is double when the Serial Port is used in modes 1,2, or 3. **–** Not implemented,reserved for future use * –Not implemented,reserved for future use * –Not implemented reserved for future use* GF1 General purpose flag bit GF0 General purpose flag bit PD Power Down bit. Setting this bit activates Power Down operation in the 8051BH. IDL Idle Mode bit Setting this bit activates Idle Mode operation in the 8051CBH. **Use of SMOD bit:** It is used to control baud rate. If Timer 1 is used to generate baud rate and SMOD=1, the baud rate is double when the serial port is used in modes 1, 2, or 3**.**	**Format 3M** **Use 1M**
	d)	**Draw Interfacing Diagram of LCD display with 8051. Write function of RS and Enable pins.**	**4M**

	Ans:	**Diagram:**  Interfacing 16x2 LCD module to 8051 **RS:** RS is the register select pin. We need to set it to 1, if we are sending some data to be displayed on LCD. And we will set it to 0 if we are sending some command instructions during the initializing sequence like clear the screen etc. **EN:** The enable pin is used by the LCD to latch information presented to its data pins. When data is supplied to the data pins, a high-to-low pulse must be applied to this pin in order for the LCD to latch in the data present at the data pins. This pulse must be a minimum of 450ns wide.	**2M for diagram** **2M for function of two pins (1M each pin function)**
Q.3		**Attempt any THREE of the following :**	**12- Total Marks**
	a)	**Explain power saving modes of 8051 µc.**	**4M**

Ans:



Two Power saving options in 8051 are Power down mode and Idle Mode

Power Down mode: (1 Mark)

- By setting the PD bit of the PCON register from within the program, the microcontroller is set to Power down mode.
- Thus turning off its internal oscillator reduces power consumption enormously.
- The microcontroller can operate using only 2V power supply in power- down mode, while total power consumption is less than 40uA.
- The only way to get the micro controller back to normal mode is by reset.

- While the microcontroller is in Power Down mode, the state of all SFR registers and I/O ports remains unchanged.
- By setting it back into the normal mode, the contents of the SFR register is lost, but the content of internal RAM is saved.

Idle Mode (1 Mark)

- Upon the IDL bit of the PCON register is set, the microcontroller turns off the greatest power consumer- CPU unit while peripheral units such as serial port, timers and interrupt system continue operating normally consuming below 6.5mA.

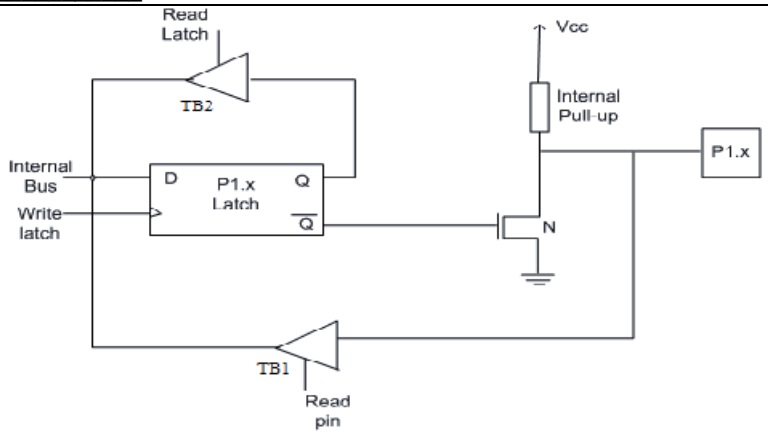
- In Idle mode, the state of all registers and I/O ports remains unchanged.

- In order to exit the Idle mode and make the microcontroller operate normally, it is necessary to enable and execute any interrupt or reset.

Diagram (1 Mark), List (1 Mark), Explanation(1 Mark each)

	b)	**List any four addressing modes with suitable example.**	**4M**
	Ans:	1. **Immediate addressing mode**: In this type of addressing mode, directly data is given to instruction to perform operation. A special character '#' is used to differentiate data from addresses. Example: MOV A , #20H ; this instruction means move data 20H to register A **2. Register Addressing Mode** In this type of addressing mode, one of the register of 8051 is specified as operand. Example: MOV R0 , A ; it means data is moved from register A to register R0. However the data is not removed from A register, it is just copied. **3. Direct Addressing** In Direct Addressing Mode, the address of the data is specified as the Operand in the instruction. Using Direct Addressing Mode, we can access any register or on-chip variable. This includes general purpose RAM, SFRs, I/O Ports, Control registers. Example MOV A,30H, Here, the data in the RAM location 30H is moved to the Accumulator. **4. Register Indirect Addressing** In the Register Indirect Addressing Mode, the address of the Operand is specified as the content of a Register. Only R0 and R1 are allowed as memory pointers in Indirect Addressing Mode. The @ symbol indicates that the addressing mode is indirect **Example:** MOV A,@R1. If the contents of R1 is 30H, then the operand is in the internal RAM location 30H. If the contents of the RAM location 30H is 24H, then 24H is moved into accumulator. **5. Indexed Addressing Mode** With Indexed Addressing Mode, the effective address of the Operand is the sum of a base register and an offset register. The Base Register can be either Data Pointer (DPTR) or Program Counter (PC) while the Offset register is the Accumulator (A). .**Example: MOVC A,@A+DPTR Here, the address for the operand is the sum of contents of DPTR and Accumulator.**	
	c)	**Describe the function of following instructions of 8051.** **i) SWAP A** **ii) MOVC A, @ DPTR** **iii) ADD A @ Ro** **iv) INC @ Ro**	**4M**

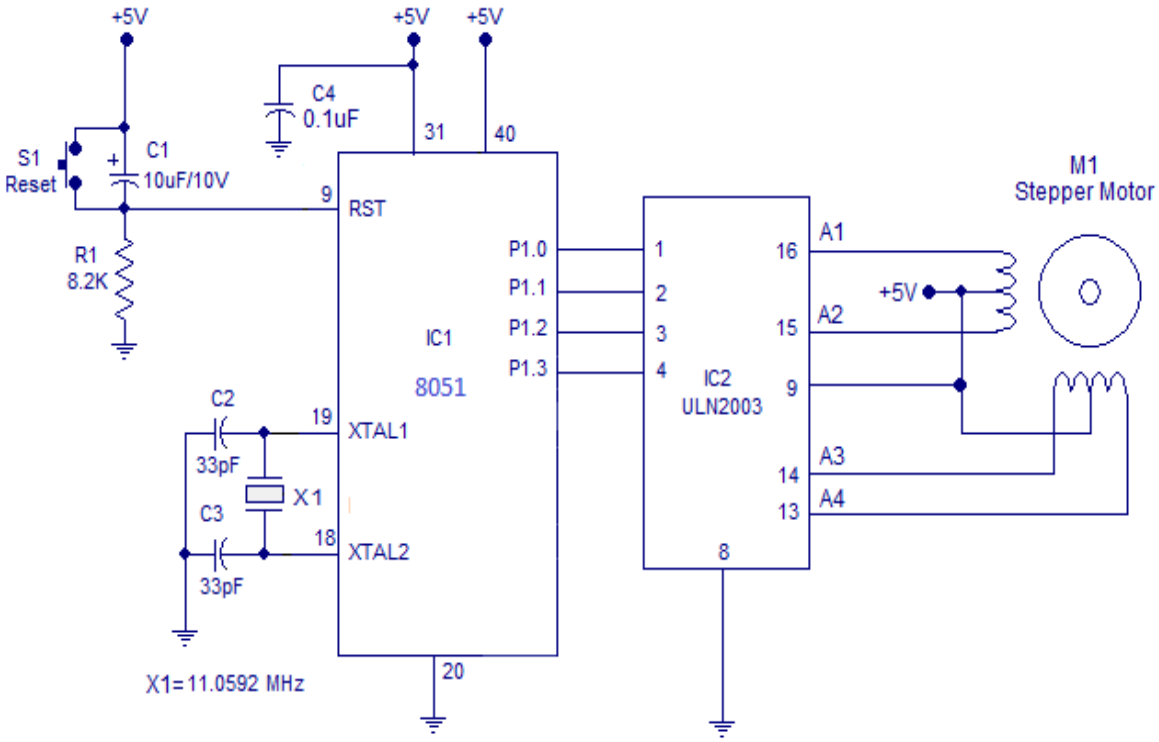
	Ans:	**i) SWAP A:** The **SWAP** instruction exchanges the low-order and high-order nibbles within the accumulator. For Example if the data in accumulator is 57H, after execution of SWAP A instruction, it becomes 75H **ii) MOVC A,@A+DPTR (the instruction MOVC A,@DPTR is not there in the instruction set of 8051) :** MOVC moves a byte from Code Memory into the Accumulator. The Code Memory address from which the byte will be moved is calculated by summing the value of the Accumulator with DPTR. **NOTE: Marks may be given to any other relevant answers** **iii) ADD A,@R0 :** This instruction will add the contents of memory location whose address is pointed by register R0 of the selected register bank with contents of the accumulator. The result of addition is stored in the accumulator. **iv) INC @R0:** This instruction will increment the contents of memory location that is pointed by register R0 by 1	**1 Mark for each instruction**
	d)	**Draw internal structure of Port 1 and explain it.**	**4M**

	Ans:	 P1 is a true I/O port as it doesn't have any alternative functions as in P0, but this port can be configured as general I/O only. It has a built-in pull-up resistor and is completely compatible with TTL circuits. The internal structure of Port 1 consists of a D Latch, two buffers and a FET. If we want to write 1 on pin of Port 1, a '1' written to the latch which turns 'off' the FET . Due to Vcc connection through internal pull up resistor, the port pin will be at logic 1.When a 0 is written to the latch, the FET will be turned ON and pin will be at Logic 0. To use port-1 as input port, initially logic '1' has to be written to the latch to turn off the FET. When '1' is written to the pin by the external device then it read fine, through the Buffer TB1. But when '0' is written to the pin by the external device then the external source must sink current due to internal pull-up, otherwise the pin voltage may rise leading to a possible wrong reading.	**Diagram : 2 Marks, Explanation : 2 Marks**
Q.4		**Attempt any <u>THREE</u> of the following :**	**12- Total Marks**
	a)	**Develop a program to generate square wave on P2.7 of 8051 using software delay.**	**4M**

	Ans:	Program ORG 0000H UP: SETB P2.7 ACALL DELAY CLR P2.7 ACALL DELAY SJMP UP DELAY: MOV R1,#0FFH L1: MOV R2,#0FFH L2: DJNZ R2,L2 DJNZ R1,L1 RET END **Note: Marks may be given to any other correct program**	**Program : 4 Marks**
	b)	**Compare Harvard and Vonneuman Architecture.**	**4M**

	Ans:	<table><tr><th>VON NEUMANN ARCHITECTURE</th><th>HARVARD ARCHITECTURE</th></tr><tr><td>Same physical memory address is used for instructions and data.</td><td>Separate physical memory address is used for instructions and data.</td></tr><tr><td>There is common bus for data and instruction transfer.</td><td>Separate buses are used for transferring data and instruction.</td></tr><tr><td>Two clock cycles are required to execute single instruction.</td><td>An instruction is executed in a single cycle.</td></tr><tr><td>It is cheaper in cost and simple in design</td><td>It is costly than Von Neumann Architecture and has complex design.</td></tr><tr><td>CPU cannot access instructions and read/write at the same time.</td><td>CPU can access instructions and read/write at the same time.</td></tr><tr><td>Examples of Von – Neumann Architecture: ARM 7 and Pentium Processors etc..</td><td>Examples of Harvard Architecture: 8051, ARM 9, AVR by Atmel Corporation and PIC microcontrollers by microchip Technology etc</td></tr></table>	**Any Four Points – 1 Mark each**
	c)	**Draw the interfacing diagram of stepper motor with 8051 microcontroller. Write an ALP to rotate a stepper motor counter clockwise by 360**	**4M**

Ans:



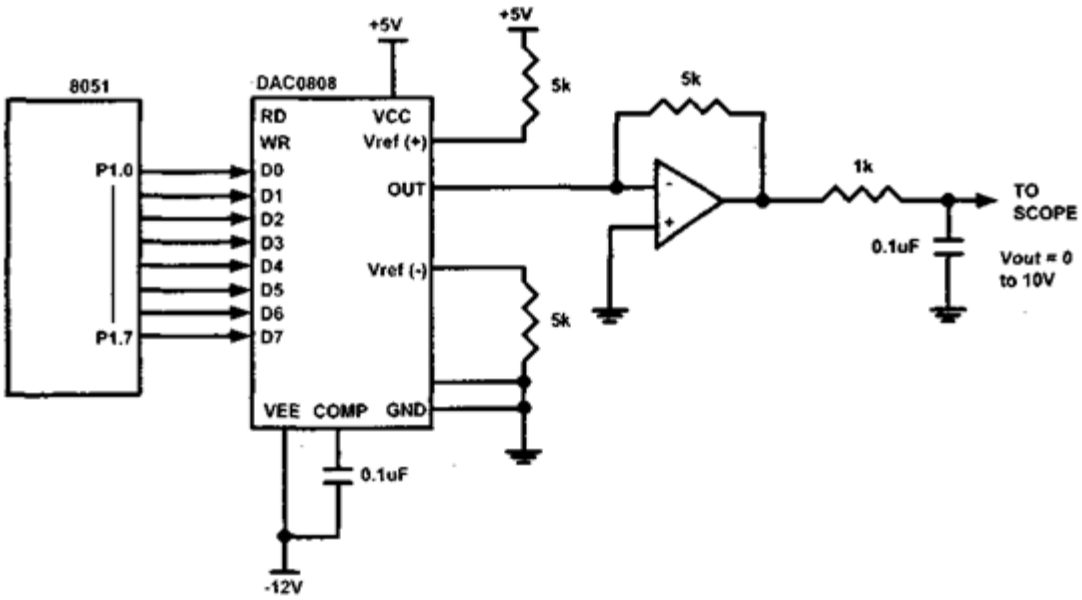
Note: Marks may be given to any other correct diagram.

Step angle = 1.8^0, Number of steps required = 360/1.8 = 200d =C8H

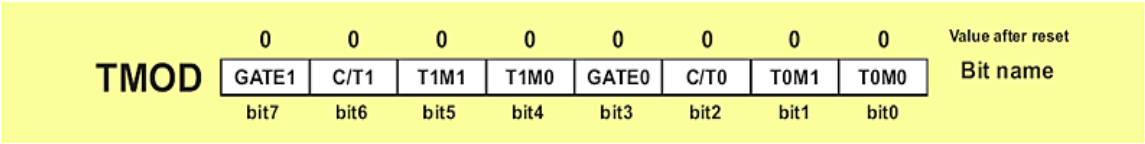
```
ORG 0000H
MOV R0,#0C8H
MOV A,#99H
L1: MOV P1,A
ACALL DELAY
RL A
DJNZ R0,L1
DELAY:   MOV R7,#4
WAIT2:  MOV R6,#0FFH
WAIT1:  MOV R5,#0FFH
WAIT:   DJNZ R5,WAIT
DJNZ R6,WAIT1
DJNZ R7,WAIT2
RET
END
```

Note: Marks may be given to any other correct program

Interfacing Diagram – 2 Marks, Program – 2 Marks

	d)	**Draw the interfacing diagram of DAC with 8051 microcontroller.** **Write an ALP to generate a square waveform.**	**4M**
	Ans:	 **Program for square waveform:** ORG 0000H CLR A LOOP1: MOV P1,A CPL A ACALL DELAY SJMP LOOP1 DELAY: MOV R7,#4 WAIT2: MOV R6,#0FFH WAIT1: MOV R5,#0FFH WAIT: DJNZ R5,WAIT DJNZ R6,WAIT1 DJNZ R7,WAIT2 RET END **Note: Marks may be given to any other correct program**	**Interfacing Diagram : 2 Marks, Program : 2 Marks**

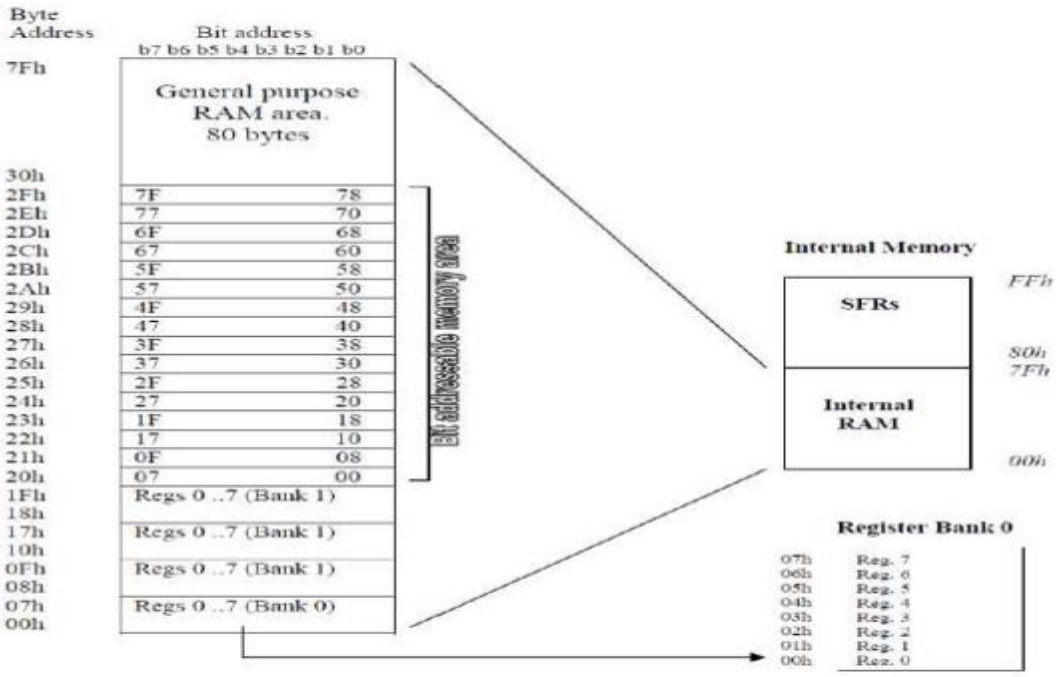
	e)	**Write an ALP to generate 1 ms delay. Use Timer 0, mode 1. Fosc =12 MHz.**	**4M**

	Ans:	**Count calculation:**
		Given Fosc-12 MHz, Required Delay = 1 ms
		Time period of Timer input Clock = 12/12 = 1microseconds
		(65535-count+1) X 1 us = 1 ms = 1000 us
		65536-count = 1000 us / 1 us = 1000
		Count = 65536 – 1000 = 64536 which in hex is FC18H
		TMOD Register:
		 
		
		To Configure Timer0 in Mode 1, the value to be given to TMOD is = 00000001 = 01H
		Program:
		MOV TMOD,#01 ;Timer 0, 16-bitmode
		MOV TL0,#18H ;TL0=18, low byte of timer
		MOV TH0,#0FCH ;TH0=FC, the high byte
		SETB TR0 ;Start timer 0
		BACK: JNB TF0,BACK ;until timer rolls over
		CLR TR0 ;Stop the timer 0
		CLR TF0 ;Clear timer 0 flag
		RET
			Count Calculation: 1 Mark, TMOD format: 1 Mark, Program: 2 Marks

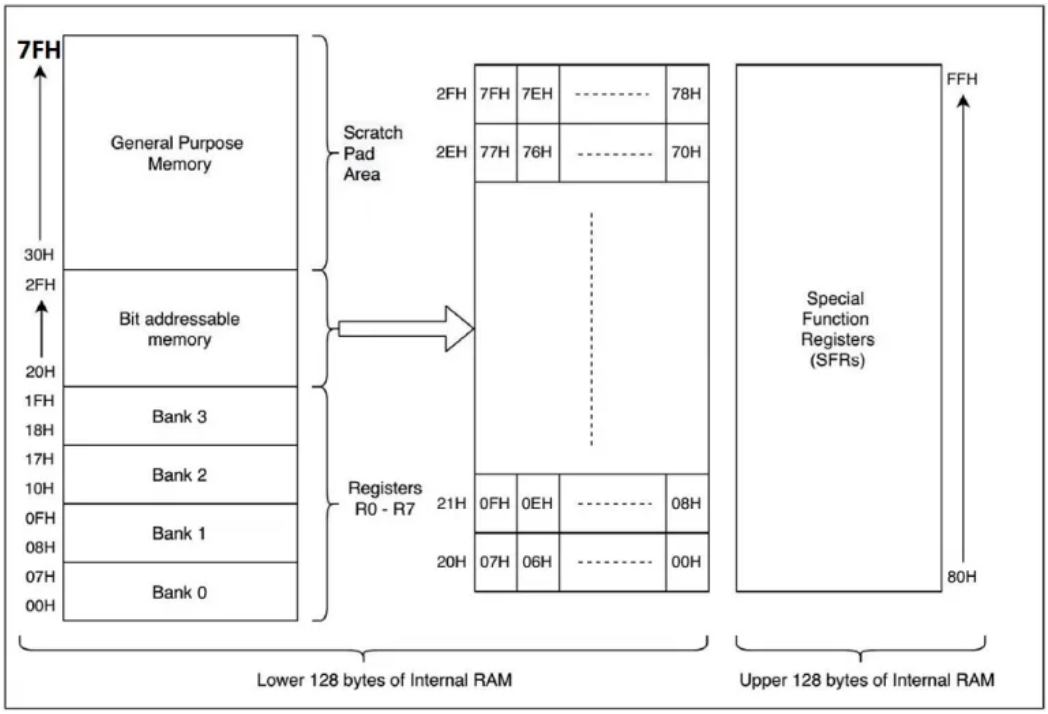
Q.5		**Attempt any TWO of the following :**	**12- Total Marks**
	a)	**Sketch memory organization of 8051 and label it showing register banks, bit addressable locations SFR area, external data and code memory.**	**6M**

Ans:

Memory organization: Internal memory:

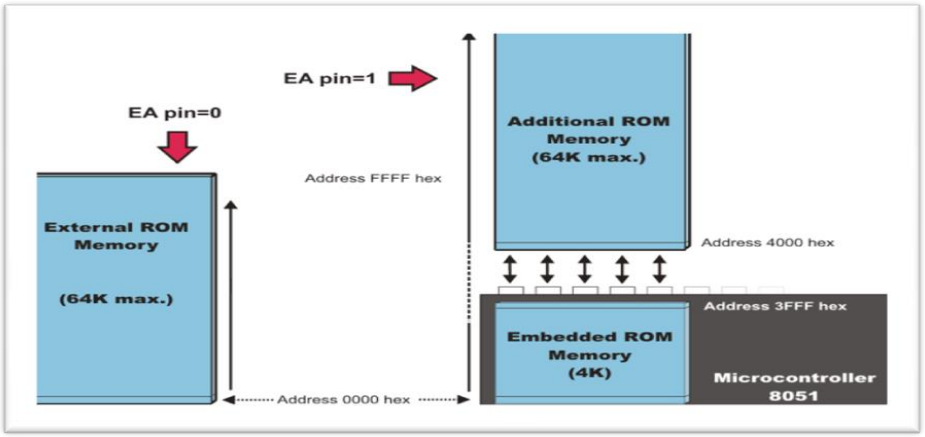


OR



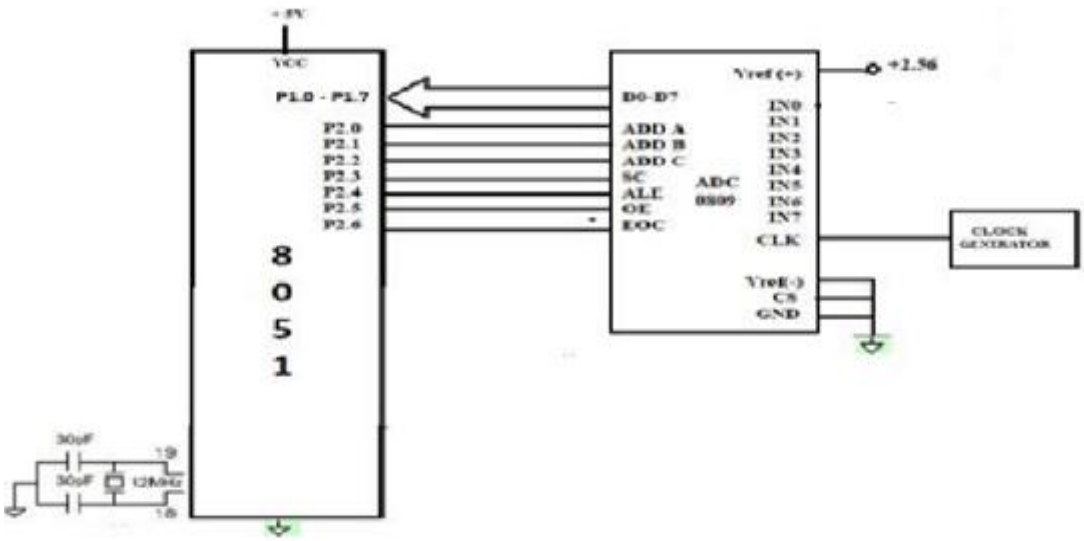
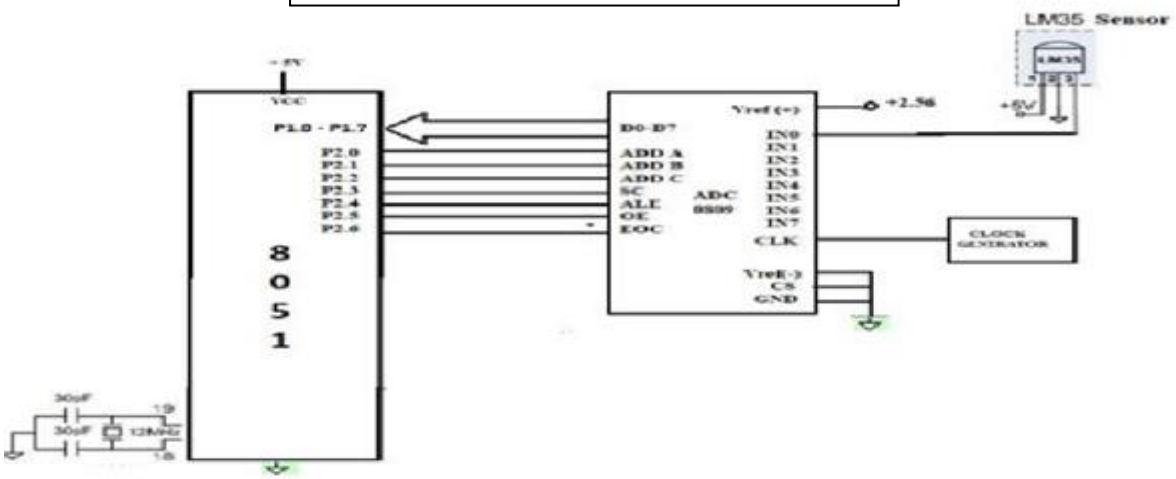
2M for diagram, 1/2M each for register banks, bit address able location s, SFR area, General purpose area labeling, 2M for Externa l code memory circuit. Marks can be given for any other relevant diagram with proper labeling.

External code memory:



	b)	**Write an ALP to find smallest no. from given array of 10 bytes in external RAM 3000h onward.**	**6M**

	Ans:	ORG 0000H
		MOV DPTR,#3000H;initialize pointer to memory where numbers are stored
		MOV R0,#0AH ; initialize counter
		MOV R3,#00H ;maximum=0
		AGAIN: MOV A,@DPTR ;get the number from memory
		CJNE A,R3,NE ;compare number wi maximum number
		AJMP SKIP ;if equal go to SKIP
		NE: JNC SKIP ;if not equal check for carry, if carry go to skip
		MOV R3,A ;otherwise maximum=[[DPTR]]
		SKIP: INC DPTR ; Increment memory pointer
		DJNZ R0,AGAIN ; Decrement count, if count=0 stop otherwise go to AGAIN
		END
			(correct program or other logic 6 marks)

	c)	**Draw the interfacing diagram of ADC with 8051 microcontroller.**	**6M**
	Ans:	 **Interfacing diagram of ADC with 8051 microcontroller:**	**(diagram 6 M)**
Q.6		**Attempt any TWO of the following :**	**12- Total Marks**
	a)	**Develop an ALP to read temperature from LM35 sensor.** **Draw interfacing diagram with 8051.**	**6M**
	Ans:	**Interfacing diagram with 8051** 	**(interfacing diagram 2 M)**

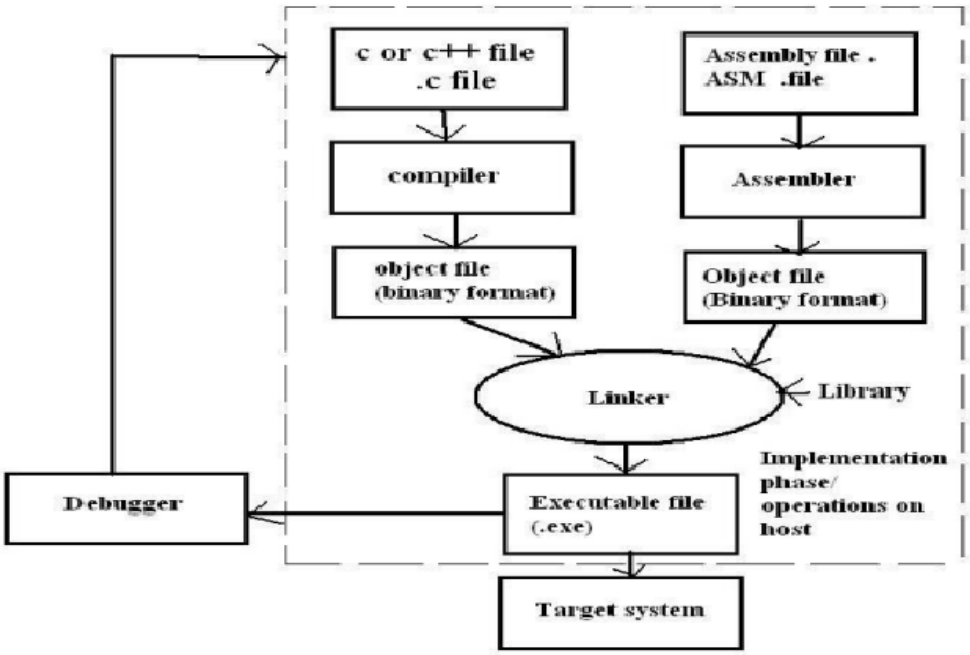
Program:

```
ORG 0000H
ADDR_A BIT P2.0
ADDR_B BIT P2.1
ADDR_C BIT P2.2
SC BIT P2.3
ALE BIT P2.4
OE BIT P2.5
EOC BIT P2.6
MY_DATA EQU P1
ORG 0000H
MOV MY_DATA,#0FFH ; make P1 as input
SETB EOC ; make EOC an input
CLR ALE ; clear ALE
CLR SC ; clear SC
CLR OE ;clear OE
CLR ADDR_C ; C=0
CLR ADDR_B ; B=0
CLR ADDR_A ; A=0(select channel 0)
ACALL DELAY
SETB ALE ;latch address
ACALL DELAY
BACK: SETB SC ;start conversion
ACALL DELAY
CLR ALE
CLR SC
HERE: JB EOC,HERE ; wait
HERE1: JNB EOC,HERE1
SETB OE
ACALL DELAY
MOV A, MY_DATA
MOV P1, A
CLR OE
SJMP BACK
DELAY: MOV R3,#25 ;Delay Subroutine
L3: MOV R4,#100
L2: MOV R5,#100
L1: DJNZ R5,L1
DJNZ R4,L2
DJNZ R3,L3
RET
END
```

program 4M

	b)	**Write an ALP to transmit 'YES' on TXD.** **Fosc=11.0592 MHz and Baud Rate=9600 bps.**	**6M**

	Ans:	**XTAL = 11.592 MHz**
		Machine Cycle freq. = 11.592 MHz/12 = 921.6 KHz.
		UART freq. = 921.6KHz/32 = 28,800 Hz. a. 28,800/3 = 9600,
		so -3=FDH is loaded to TH1 for 9600 Baud Rate
		Program:
		ORG 0000H
		MOV TMOD, #20H
		MOV TH1,#0FDH ; 9600 baud rate
		MOV SCON, #50H ; 8-bit data,1 stop bit, REN enabled
		SETB TR1 ; Start timer 1
		AGAIN: MOV A #"Y" ; transfer "Y"
		ACALL MESSAGE
		MOV A #"E" ; transfer "E"
		ACALL MESSAGE
		MOV A #"S" ; transfer "S"
		ACALL MESSAGE
		SJMP AGAIN
		MESSAGE: MOV SBUF, A
		JNB TI, $
		CLR TI
		RET
		END
			2M- TH1 calculation
			4M - program or any other correct program

	c)	**Draw software development cycle and write function of it's components.**	**6M**
	Ans:	 **Fig: software development cycle** **The Steps For the software development cycle are:** 1.Define the processor or processing device family as well as various versions for the target system. 2.Define Source code windows i.e detail information of source code with labels and symbolic arguments as execution goes on for each single step. 3.Define the processor registers i.e detail information of the registers as the execution goes on for each step or for each single module. 4. Define detail information of Ports and target system 5.Editor to edit source code files initial data files,data and tables 6.Define assembler or compiler for the program test with link library. 7.Finally execute source code to check either target system is working properly or not. 8.If the system is not working properly as per the specification then debug the source code. 9.If system is working properly as per specification the final implementation is carried out. 10.Finally, application software is embedded in the system by using device programmer.	**(correct diagram 3 marks and steps 3 marks)**

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