Instructions:

(1) All questions are compulsory.
(2) Illustrate your answers with neat sketches wherever necessary.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary.
(5) Preferably, write the answers in sequential order.

Q.1) Attempt any FIVE of the following :- 10 Marks (5X2)

(a) Draw the symbol and write the truth table of Universal Gates.
(b) In a 3 variable K’ Map if there are two quads, interpret the simplified output.
(c) Define modulus of counter and write down the number of flips flops required to construct mod 7 counter
(d) Construct OR gate using NOR gate.
(e) Identify the addressing mode of the instruction: MOV A, @R0 and DJNZ Rn, rel
(f) Demonstrate with example the function of EQU directive.
(g) Find the number of address lines required for:
   1. 2K RAM
   2. 16K ROM

Q.2) Attempt any THREE of the following :- 12 Marks (3X4)

(a) Justify with the help of suitable diagrams ‘ NAND gate is a universal gate.’
(b) Design Full Adder using K’map and truth table.
(c) Explain with help of waveform the Race around condition in JK flip flop. Suggest a suitable method to overcome the drawback.
(d) Compare TTL, CMOS and ECL on following points:
   1. Propagation delay
2. FAN IN
3. FAN OUT

Q.3) Attempt any THREE of the following. 12 Marks (3X4)

(a) List the various stages in software development cycle and explain importance of each stage.
(b) Interface Steeper motor to 8051 and write an ALP to rotate Stepper motor in clockwise direction.
(c) Simplify the following using K’ Map and implement using NAND-NAND gates only:
   \[ Y = \Sigma m(0,1,2,3,5,7,8,9,11) \]
(d) Draw the architecture of 8051 and label various blocks.

Q.4) Attempt any THREE of the following. 12 Marks (3X4)

(a) Explain the meaning of following instructions:
   1. MOV A, FOH
   2. ADD A, R4
   3. SWAP A
   4. CJNE R1, #data, rel
(b) Execute the following program and specify the contents of Accumulator and status of PSW after execution:
   MOV A, #23H
   MOV 0F0H, #02H
   MUL AB
   END
(c) Identify the given circuit in Fig 1 and write its truth table:

![Fig 1](image)

(d) Apply Boolean rules to simplify the following:
   1. \[ Y = A\overline{B} + \overline{A}B + AB + \overline{A}\overline{B} \]
   2. \[ Y = \overline{A}\overline{B}C + \overline{A}BC + ABC \]
(e) Which pins of 8051 are used to perform the following functions:
1. Receive the serial data
2. Enable of external memory.
3. Multiplexing and de-multiplexing of address/ data lines.
4. Applying external interrupts.

Q.5) Attempt any TWO of the following. 12 Marks (2x6)
   (a) Develop an ALP to generate a square wave with ON time of 7 msec and OFF time of 3 msec.
   (b) Write an ALP to find average of ten, 8 bit numbers stored in internal memory location starting from 40H and store the result in 70 H location.
   (c) Explain the various power saving options of 8051.

Q.6) Attempt any TWO of the following. 12 Marks (2x6)
   a) Identify the special function registers(SFR ) to do the following:
      1. Change the priorities of various interrupts in 8051.
      2. Enabling and disabling of various interrupts in 8051.
      Explain bit functions of each bit of these SFRs.
   b) Develop an ALP to turn ON/OFF the relay. Draw suitable interfacing diagram
   c) Construct 3 bit asynchronous up counter using flip flop. Draw its timing diagram
Scheme – I

Sample Test Paper - I

Program Name : Electrical Engineering Program Group
Program Code : EE/EP/EU
Semester   : Fourth
Course Title    : Digital Electronics and Microcontroller Applications
Marks : 20

Time: 1 Hour

Instructions:

(1) All questions are compulsory.
(2) Illustrate your answers with neat sketches wherever necessary.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary.
(5) Preferably, write the answers in sequential order.

Q.1 Attempt any FOUR. 08 Marks (4X2)

a) Define the characteristics of logic families:
   1. Speed of operation.
   2. Power dissipation.

b) Draw the symbol and write truth table of EX OR gates.

c) State the cumulative and associative law for Boolean algebra.

d) Write the excitation table for D flip flop.

e) State the need of De-multiplexer.

f) Define min-term and max-term.

Q.2 Attempt any THREE. 12 Marks (3X4)

(a) Simplify using K’ Map and implement using NOR- NOR gates only:
   \[ f( A,B,C,D)= \pi M (0,2,6,7,8,10,12,14,15) \]

(b) Explain the operation of SR Flip Flop and draw its truth table.

(c) Prove NOR gate as universal gate with suitable diagrams.

(d) Implement mod 7 asynchronous down counter and draw suitable waveforms.
Instructions:

(1) All questions are compulsory.
(2) Illustrate your answers with neat sketches wherever necessary.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary.
(5) Preferably, write the answers in sequential order.

Q.1 Attempt any FOUR. 08 Marks (4X2)

(a) List the functions of address and Data Bus.
(b) Classify the following applications under Von-Neuman and Harvard Architecture:
   i. Digital Signal Processing.
   ii. 8051 Microcontroller
(c) Illustrate the functions of Editor and Complier.
(d) List the alternate functions of Port 3 of 8051.
(e) Calculate size of memory if number of address lines for a memory chip are 12 and data bus width is of 8 bit.
(f) List any four addressing modes of 8051 with one example of each,

Q.2 Attempt any THREE. 12 Marks (3X4)

a) Develop an ALP to find the largest number out of ten numbers stored from internal memory location 60H onwards and store the result at 70H memory location.
b) Draw an interfacing diagram of 8 LEDs connected to port 2 of 8051 and write a program to toggle LEDs after 100 msec delay.
c) Compare microcontroller with microprocessor on the basis of any four factors.
d) Draw the interfacing diagram of Traffic light controller with 8051.