SUMMER – 2022 EXAMINATION

Subject Name: Digital Electronics and Microcontroller Applications **Model Answer:** **22421: DEM**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.	Answer	Marking Scheme
1.		**Attempt any FIVE of the following:**	**10 Marks**
	a)	State 1. Duality Theorem 2. De-Morgan's Theorem **Ans:** **i)Duality Theorem :** Duality theorem states that the dual of the Boolean function is obtained by interchanging the logical AND operator with logical OR operator and zeros with ones. For every Boolean function, there will be a corresponding Dual function. For ex $x + 0 = x \rightarrow x.1 = x$ **ii)De-Morgan's Theorem** **De-Morgan's first theorem-** It states that the complement of a product is equal to the sum of the individual complements. Or This theorem states that the complement of a product of variables is equal to the sum of their individual complements. i.e. $\overline{A.B} = \overline{A} + \overline{B}$ **De-Morgan's second theorem-** It states that the complement of a sum is equal to the product of the complements. Or This theorem states that the complement of a sum of variables is equal to the product of their individual complements. i.e. $\overline{A+B} = \overline{A}.\overline{B}$	1 marks 1 marks
	b)	Draw symbol and truth table of Universal Gates. **Ans:**	

i] NAND GATE

Symbol

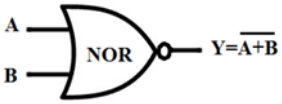
Truth table:

Inputs		Output
A	B	$Y=\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

1 marks (½ mark for symbol & ½ mark for truth table)

ii] NOR GATE

Symbol



Truth table:

Inputs		Output
A	B	$Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

1 marks (½ mark for symbol & ½ mark for truth table)

c) State race around condition in JK flip flop.

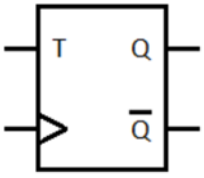
Ans:

For J-K flip-flop, if J=K=1, and if CLK =1 for a long period of time, then output Q will toggle as long as CLK remains high which makes the output unstable or uncertain. This condition is called as race around condition in JK flip-flop. 2 marks

d) Draw symbol and truth table of T type flip flop.

Ans:

Symbol



Truth table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

OR

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

1 mark for symbol & 1 mark for truth table

e) Explain assemble directives.

i] DB

ii] EQ

Ans:

i] DB

Define Byte - This directive is used for the purpose of allocating and initializing single or multiple data bytes.

```
AREA DB 30H, 52H, 35H
```

Memory name AREA has three consecutive locations where 30H, 52H and 35H are to be stored.

1 mark for each directives

ii] EQ

Equate- It is used to assign any numerical value or constant to the variable.

```
DONE EQU 10H
```

A value 10H is assigned to variable name 'DONE'.

f) Explain PUSH instruction with one example

Ans:

This instruction increments the stack pointer (SP) by 1. The contents of Direct, which is an internal memory location or a SFR, are copied into the Stack Memory (Top of the stack) by the stack pointer.

Operation : SP = SP + 1
Content of direct address /SFR ➔ TOS
No of byte : 1 byte or 2 byte
Addressing mode : register / direct addressing
Effect on flag: No effect on Flag (only data transfer).

1 mark For Correct Explanation

Example:
Let SP =0AH and data pointer = 1234H
PUSH DPL
PUSH DPH
The first instruction PUSH DPL will set the SP = 0BH and store 34H in internal RAM location 0BH.
The second instruction PUSH DPH will set the SP = 0CH and store 12H in internal RAM location 0CH.
The stack pointer will remain at 0CH.

1 marks for any correct example

(Note : Any other correct definition and example may please be considered)

g) State the function of LCD display pins.
i) R/W
ii) RS

Ans:

i] R/W - Read/Write/Control Pin :

This pin toggles the display among the read or writes operation, and it is connected to a microcontroller to get either 0 or 1
(0 = Write Operation, and 1 = Read Operation).

Or

When R/W = 0 its write operation
R/W = 1 its read operation

1 mark

ii] RS - Register Select/Control Pin :

This pin toggles among command or data register, used to connect a microcontroller unit pin and obtains either 0 or 1(1 = data mode, and 0 = command mode).

Or

RS: its register select pin .

It select Data register or command register depending on the status of RS bit
If RS = 0 it will select the Command Register
If RS = 1 it will select the data register — 1mark

2. Attempt any THREE of the following: **12 Marks**

a) Compare between TTL and CMOS. (any four points).

Ans:

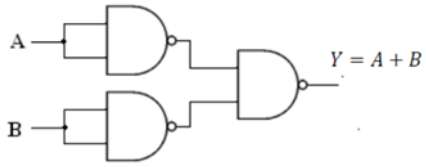
TTL	CMOS
1. TTL stand for Transistor-Transistor Logic.	1. CMOS stands for Complimentary Metal-oxide Semiconductor
2. TTL circuit uses bipolar junction transistor.	2. CMOS circuit uses a field-effect transistor by connecting NMOS and PMOS
3. The design of the TTL is quite complex.	3. The design of the CMOS is simple.
4. Fan-in for TTL is 12-14.	4. Fan-in for CMOS is 10.
5. Propagation delay for TTL is 10ns	5. Propagation delay for CMOS is 20-50ns
6. Fan-out for TTL is 10	6. Fan-out for CMOS is 50
7. Power dissipation in TTL is 10mW	7. Power dissipation in CMOS is 1.01mW
8. Figure of merit is 100pJ	8. Figure of merit is 0.7pJ
9. Clock rate for TTL is 35MHz	9. Clock rate for CMOS is 10MHz
10. Supply voltage is fixed 5V	10. Supply voltage is variable between 3V to 15 V

1 mark for each of any four points = 4 marks

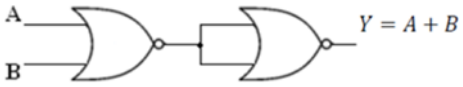
b) Draw OR gate and AND gate using universal gates.

Ans:

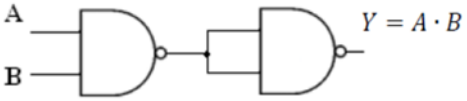
i] OR gate using NAND gate — 1 mark



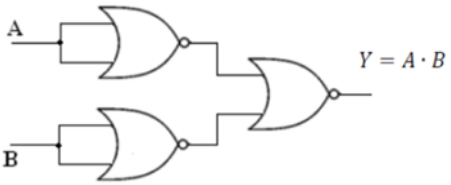
ii] OR gate using NOR gate — 1 mark



iii] AND gate using NAND gate — 1 mark

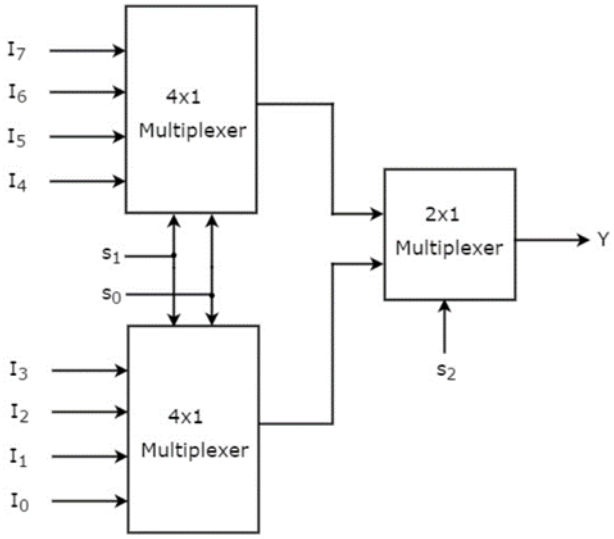


iv] AND gate using NOR gate — 1 mark



c) Design 8:1 MUX using 4:1 & 2:1 MUX. Draw Truth Table.

Ans:



2 marks for diagram & 2 marks for truth table

Truth table

Selection Inputs			Output
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

d) Minimise the following Boolean expression using K-Map and realize it using the basic logic gates.

Ans:

Boolean expression is not given, so cannot solve the example.

3. Attempt any THREE of the following: **12 Marks**

a) Explain any four addressing modes of 8051 with one example each.

Ans:

1. Immediate addressing mode: In this Immediate Addressing Mode, the data is provided in the instruction itself. The data is provided immediately after the opcode.

Immediate data is given in the instruction.

These are some examples of Immediate Addressing Mode.

MOV R2, # 35H

MOV A, #0AFH;

1 marks For each Mode

2. Register addressing mode: In the register addressing mode the source or destination data should be present in a register (R0 to R7). These are some examples of Register Addressing Mode. (½ Marks Definition ½ Mark Example)

```
MOV  A, R5;
MOV  R0, A;
```

3. Direct Addressing Mode: In the Direct Addressing Mode, the source or destination address is specified in the instruction. Only the internal data memory can be used in this mode. Here some of the examples of direct Addressing Mode.

```
MOV   80H, R6;
MOV   R2, 45H;
MOV   R0, 05H;
JMP 3000H
```

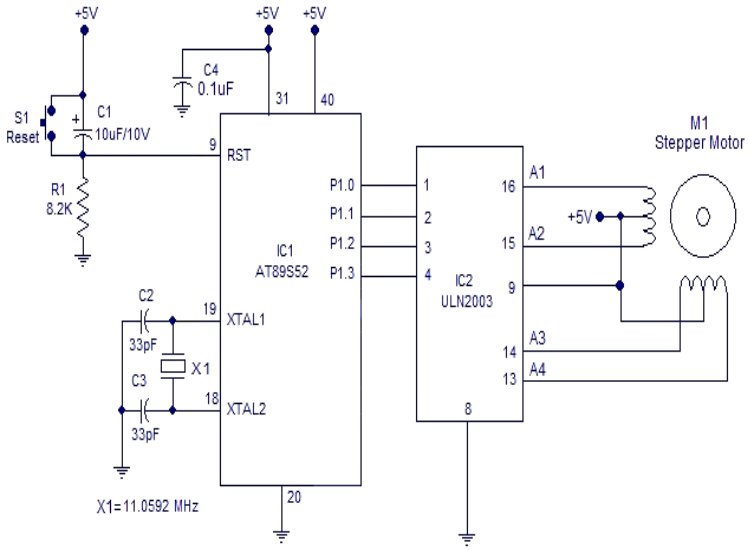
4. Register indirect addressing Mode: In this mode, the source or destination address is given in the register. By using register indirect addressing mode, the internal or external addresses can be accessed. The R0 and R1 are used for 8-bit addresses, and DPTR is used for 16-bit addresses, no other registers can be used for addressing purposes.

Address is indirectly given in instruction.
Example:

```
MOV A, @R0
MOV @R1, A
```

b) Interface stepper motor to 8051microcontroller and write an ALP to rotate stepper motor in anti-clockwise direction continuously.

Ans :



2 marks for diagram

```
ORG 0000H
  MOV P1, #00H;          Make Port P1 as Output port
  MOV A, #0CCH ;         load step sequence
  BACK: MOV P1, A        Send this step sequence to port P1 .
  ACALL DELAY ;          Give some delay
```

```
        RL A ;              rotate Left  (Anticlockwise )
        SJMP BACK ;         keep doing
```

2 marks for Correct Program

```
        //Delay subroutine.
DELAY :  MOV R2,#64H
    H1:  MOV R3,#0FFH
    H2:  DJNZ R3, H2
         DJNZ R2, H1
         RET
         END
```

(Note : Students can use any step sequence and delay routine. Any other correct program /diagram may please be considered)

c) Compare between combinational and sequential circuits.(any four points)
Ans:

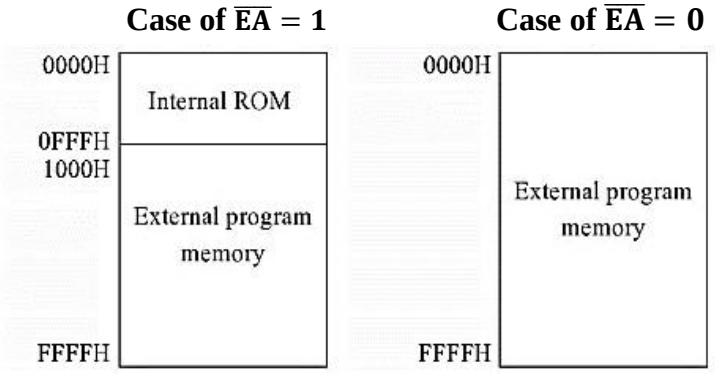
Parameters	Combinational Circuit	Sequential Circuit
Meaning and Definition	It is a type of circuit that generates an output by relying on the input it receives at that instant, and it stays independent of time.	It is a type of circuit in which the output does not only rely on the current input. It also relies on the previous ones.
Feedback	A Combinational Circuit requires no feedback for generating the next output. It is because its output has no dependency on the time instance.	The output of a Sequential Circuit, on the other hand, relies on both- the previous feedback and the current input. So, the output generated from the previous inputs gets transferred in the form of feedback. The circuit uses it (along with inputs) for generating the next output.
Performance	We require the input of only the current state for a Combinational Circuit. Thus, it performs much faster and better in comparison with the Sequential Circuit.	In the case of a Sequential Circuit, the performance is very slow and also comparatively lower. Its dependency on the previous inputs makes the process much more complex.
Complexity	It is very less complex in comparison. It is because it basically lacks implementation of feedback.	This type of circuit is always more complex in its nature and functionality. It is because it implements the feedback, depends on previous inputs and also on clocks.
Elementary Blocks	Logic gates form the building/ elementary blocks of a Combinational Circuit.	Flip-flops form the building/ elementary blocks of a Sequential Circuit.

1 Mark for each of any points = 4 Marks

Operation	One can use these types of circuits for both- Boolean as well as Arithmetic operations.	You can mainly make use of these types of circuits for storing data.

d) Draw memory organization for $\overline{EA} = 0$ and $\overline{EA} = 1$ and explain the same.

Ans:



1 mark for each diagram = 2 marks

Or Equivalent diagram

$\overline{EA}$ = 0, When $\overline{EA}$ = 0 , Microcontroller access the External Program memory .

The 8051 microcontrollers ignore the internal memory and start the execution of a program stored in external memory.

2 marks for explanation

$\overline{EA}$ = 1, When $\overline{EA}$ = 1 , Microcontroller access the Internal memory

The 8051 Microcontroller executes the program form internal ROM and later the execution is continued by executing the program from additional memory.

4. Attempt any THREE of the following: **12 Marks**

a) Explain the following instructions:
(i) DAA
(ii) DIV AB
(iii)CJNE A, data, rel
(iv)SWAP A

Ans :

1) DAA

The **DA** instruction adjusts the eight-bit value in the Accumulator resulting from the earlier addition of two variables (each in packed-BCD format), producing two four-bit digits. This instruction is used only after the addition, to adjust the result of addition to BCD format, this instruction can not used after subtraction.

The data is adjusted in following possible way :

1. If lower 4 bit of accumulator is greater than 9 or if AC = 1, then it adds 6 to lower 4 bit.

1 Marks for each Instruction = 4 Marks

2. If Higher 4 bit of accumulator is greater than 9 or if CY =1, then it adds 6 to higher 4 bit.

Operation : Result in accumulator = A (BCD format)
No of byte : 1
Addressing mode : Register addressing mode
Effect on flag : CY

2) DIV AB

The DIV instruction divides the unsigned 8-bit integer in the accumulator by the unsigned 8-bit integer in register B. After the division, the quotient is stored in the accumulator and the remainder is stored in the B register. The carry and OV flags are cleared.

If the B register begins with a value of 00h the division operation is undefined, the values of the accumulator and B register are undefined after the division, and the OV flag will be set indicating a division-by-zero error.

Example : DIV AB

3) CJNE A, data, rel

When this types of instructions are executed the content of accumulator get compare with the data , the comparison is done by subtracting data from Accumulator , and if A and data are not equal then program control transfer to the relative address , relative address range is -128 to 127 only. Here it does not store the result of subtraction , only affect the carry flag in following way :

- If dest = Source byte CY = 0
- If dest > Source byte CY = 0
- If dest < Source byte CY = 1

No of byte : 3 byte
Effect on flag : CY

4) SWAP A

The SWAP instruction exchanges the low-order and high-order nibbles within the accumulator. No flags are affected by this instruction.

Operation : Lower order nibble exchange with higher order nibble of Accumulator

b) Compare Harvard and Von-Neumann architecture. (Any four points)

Ans:

VON NEUMANN ARCHITECTURE	HARVARD ARCHITECTURE
The von Neumann type of architecture has only one set of address and data bus for accessing data memory and Program memory	The Harvard type of architecture has separate set of address and data bus for accessing data memory and Program memory
Same physical memory address is used for instructions and data.	Separate physical memory address is used for instructions and data.
There is common bus for data and instruction transfer.	Separate buses are used for transferring data and instruction.
Two clock cycles are required to execute single instruction.	An instruction is executed in a single cycle.
It is cheaper in cost.	It is costly than Von Neumann Architecture.
CPU can not access instructions and read/write at the same time.	CPU can access instructions and read/write at the same time.
It is used in personal computers and small computers.	It is used in micro controllers and signal processing.

1 marks for each of any four points = 4 Marks

c) Design Half adder using K-Map and implement using basic logic gates.

Ans:

Truth table

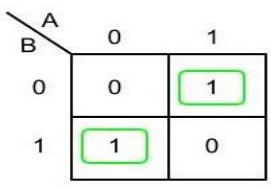
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

1 mark Truth Table

K-MAP For Sum

Sum = A'B + AB'

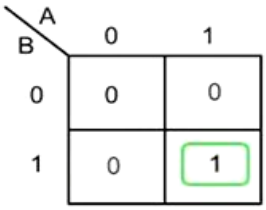
= A xor B



1 mark for K map and Expression For Sum

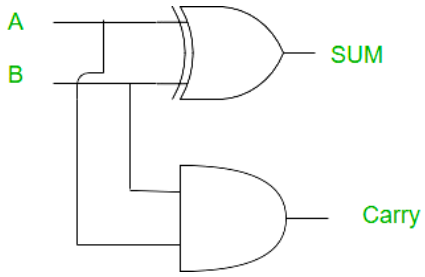
K-map for Carry

Carry = A and B



1 mark for K map and Expression For Carry

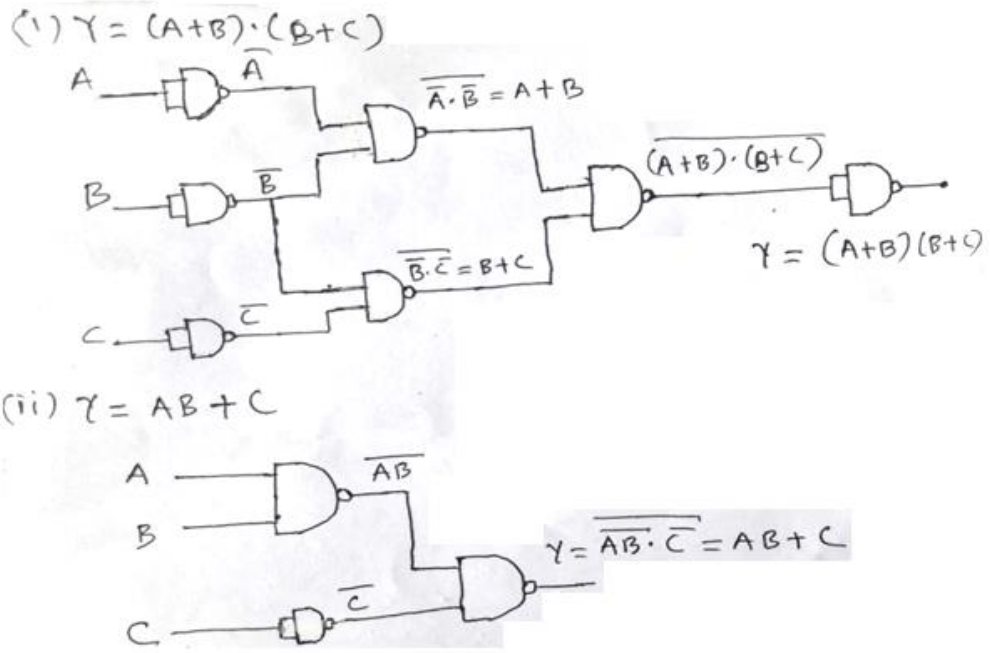
Implementation using XOR and AND Gate:



1 mark for Implementation

d) Realize the following equation using NAND gates only.

(i) Y = (A+B).(B+C)
(ii) Y = AB + C
Ans:



2 marks For Each Correct Diagram = 4 marks

(Note : Marks to be given for Any other correct Realization diagram of equation)

e) What are the alternate functions of port 3 of 8051 micro-controller?

Ans:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

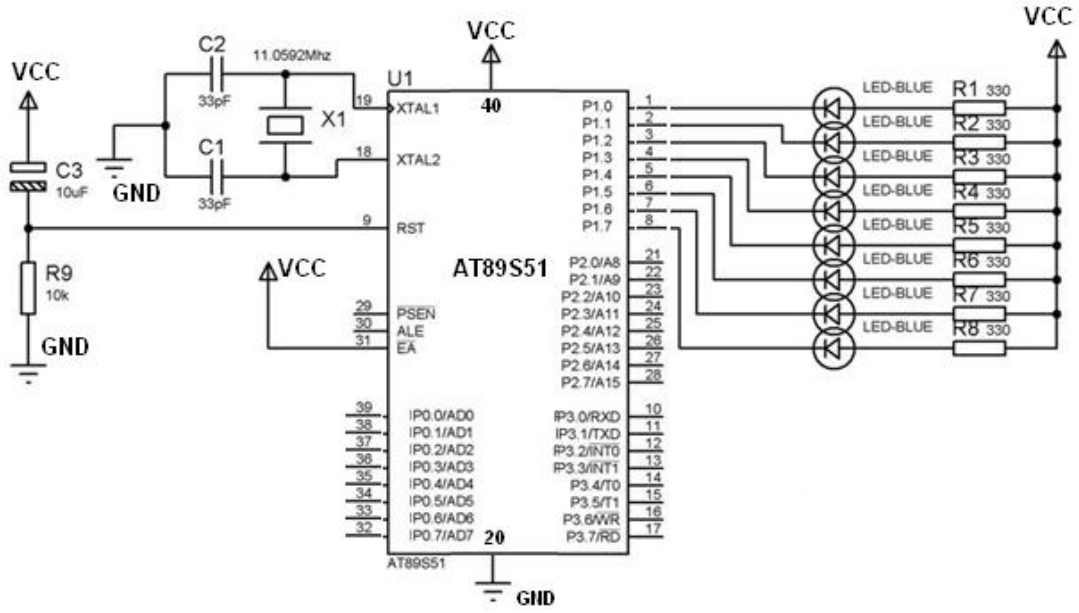
½ mark for each of eight functions = 4 marks

5 Attempt any TWO of the following: 12 Marks

5 a) Interface 8 LED's with port 1 of 8051 micro-controller. Write ALP to make LED's ON and OFF after 10 msec delays. Assume suitable data.

Ans:

Interfacing Diagram:



2 marks for Diagram

OR Equivalent diagram

10 msec delay calculation:

Assuming Crystal Freq- 11.0592 MHz 1MC= 1.085 µsec	**Assuming Crystal Freq- 12 MHz** 1MC= 1 µsec
MOV R1,#20 L2: MOV R2,# 230 L1: DJNZ R2, L1 DJNZ R1,L2 RET 20* 230* 2MC * 1.085 µsec= 10 msec	MOV R1,#20 L2: MOV R2,# 250 L1: DJNZ R2, L1 DJNZ R1,L2 RET 20* 250* 2MC * 1 µsec= 10 msec
Or assuming any other Crystal Frequency	

1 mark for Calculation

Program :

```
        MOV P1,#00h  //configure all lines of port P1 in output mode
AGAIN:  MOV P1,#00h
        ACALL DELAY
        MOV P1,#0FFh
        ACALL DELAY
        SJMP AGAIN

DELAY:  MOV R1,#20
L2:     MOV R2,# 230
L1:     DJNZ R2, L1
        DJNZ R1, L2
        RET
END
```

3 marks For program

(NOTE: Marks to be given for any other correct logic used by students.)

5 b) Develop an ALP to arrange ten numbers stored in internal memory locations starting from 40H location in descending order.

Ans:

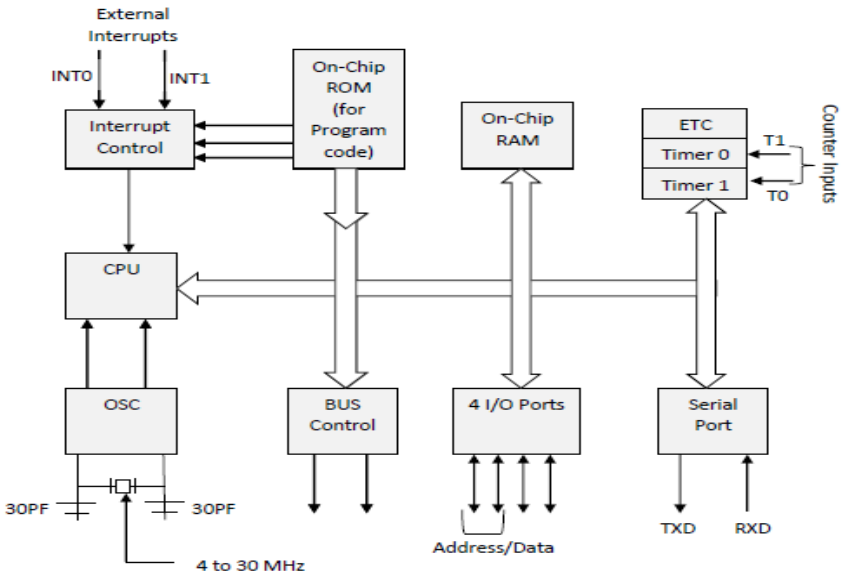
```
        ORG 0000H
        MOV R1,#09H      // Counter 1
START:  MOV R2,#09H      // Counter 2
        MOV R0,#40H      // Initialize memory pointer
        MOV A,#00H
BACK:   MOV A,@R0
        INC R0
        MOV 0F0H,@R0
        CJNE A,0F0H,LOC1  // Compare two numbers
        SJMP LOC3          //Carry will generate if A is less than B then jump else
LOC1:   JC LOC2            //Exchange
        SJMP LOC3
LOC2:   DEC R0
        MOV @R0,0F0H
        INC R0             // points to the next number
        MOV @R0,A
LOC3:   DJNZ R2,BACK       //Repeat for all numbers
        DJNZ R1,START
        END
```

6 marks For Correct Program

(NOTE: Marks to be given for any other correct logic used by students.)

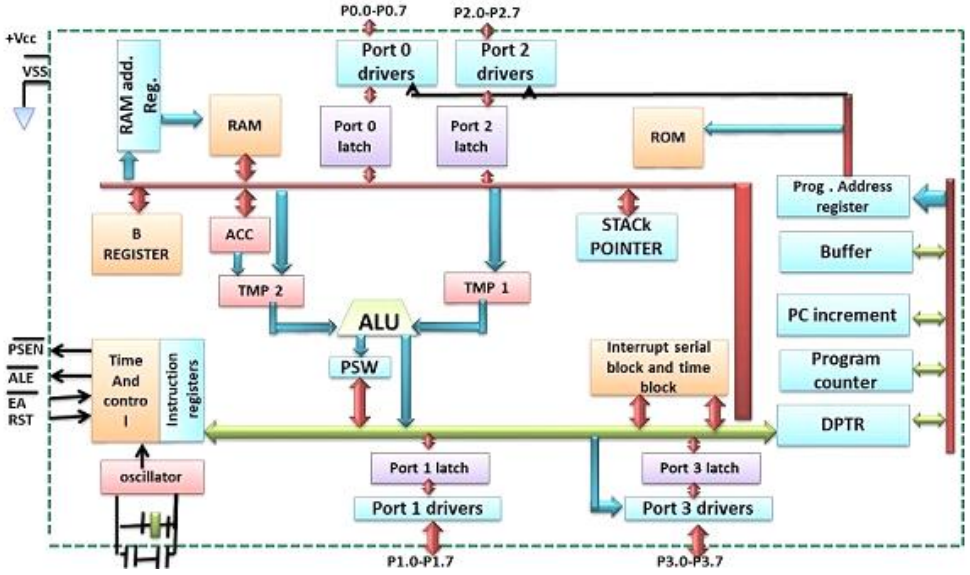
5 c) Draw architecture of 8051 Microcontroller.

Ans:



6 marks
For correct diagram

OR



OR Equivalent diagram

6 Attempt any TWO of the following: 12 Marks

6 a) Explain Power saving options
(i) Idle mode
(ii) Power down mode

Ans :

(i) Idle mode:

Idle mode is selected by setting IDL bit in PCON register.

In the Idle mode, the internal clock signal is gated off to the CPU, but not to the Interrupt, Timer and Serial Port functions.

The CPU status is preserved in its entirety, the Stack Pointer, Program Counter, Program

Status Word, Accumulator, and all other registers maintain their data during Idle

3 marks
For
Each mode
= 6 marks

mode. The port pins hold the logical state they had at the time idle mode was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the idle mode.

i) Activation of any enabled interrupt will cause PCON.0 to be cleared and idle mode is terminated.

ii) Hardware reset: that is signal at RST pin clears IDEAL bit IN PCON register directly. At this time, CPU resumes the program execution from where it left off.

(ii) Power down mode:

An instruction that sets PCON.1 causes that to be the last instruction executed before going into the Power Down mode.

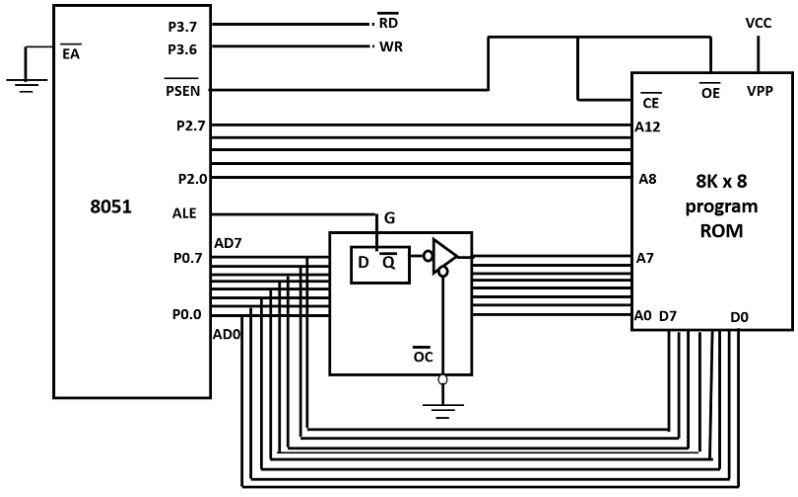
Power down mode can be selected by setting PD bit in PCON register. In the Power Down mode, the on-chip oscillator is stopped. With the clock frozen, all functions are stopped, but the content of on-chip RAM and Special Function Register are maintained. The port pins output the values held by their respective SFRS. ALE and PSEN are held low as 2 Volt.

Termination from power down mode: an exit from this mode is hardware reset.

6 b) Draw interfacing diagram of 8k × 8 program ROM with 8051 and also write memory map for same.

Ans:

Interfacing Diagram:



4 marks for Correct Diagram

Memory Map:

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
Starting Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
End address	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFH

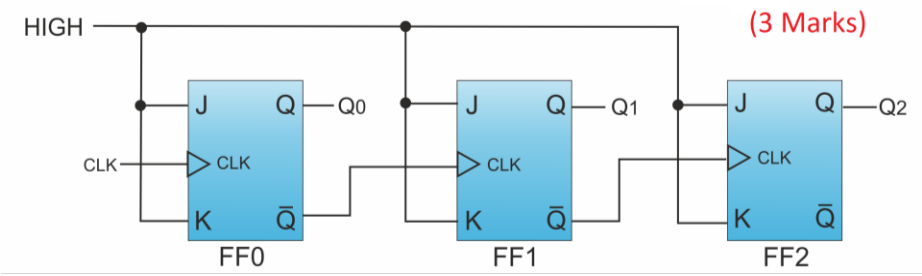
2 marks For Memory Map

(NOTE: Marks to be given for any other Correct Diagram)

6 c) Construct 3 bit asynchronous up-counter using flip-flop. Draw its timing diagram. **12 Marks**

Ans:

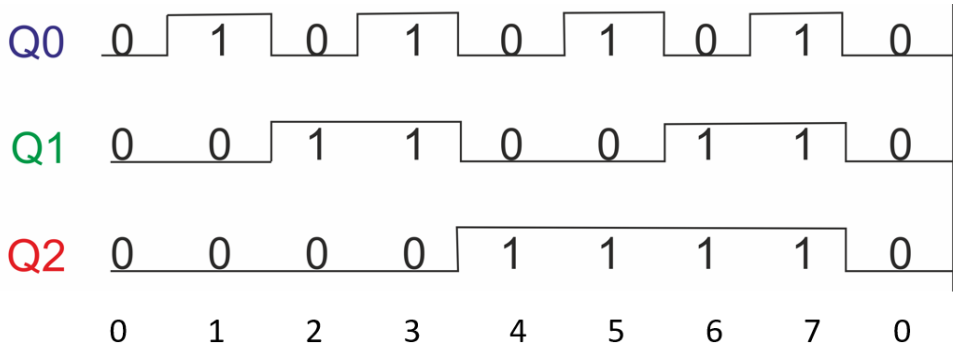
3 bit asynchronous up-counter using flip-flop:



3 marks for Correct Diagram

or Equivalent diagram

Timing diagram:



3 marks Correct Timing diagram

Note : Marks to be given to any Correct diagram using any other type of flip flop