Program Name : **Computer and Electronics Engineering Program Group**

Program Code : **CO/CM/CW/DE/EJ/ET/EN/EX/EQ/IE/IS/IC/MU**

Semester : **Third**

Course Title : **Digital Techniques**

Course Code : **22320**

1. RATIONALE

In the present scenario most of the electronic equipment like computers, mobiles, music systems, ATM, automation and control circuits and systems are based on digital circuits which the diploma electronic engineering passouts (also called technologists) have to test them. The knowledge of basic logic gates, combinational and sequential logic circuits using discrete gates as well as digital ICs will enable the students to interpret the working of equipment and maintain them. After completion of the course, students will be able to develop digital circuits based applications.

2. COMPETENCY

The aim of this course is to help the student to attain the following industry identified competency through various teaching learning experiences:

- **Build/ test digital logic circuits consist of digital ICs.**

3. COURSE OUTCOMES (COs)

The theory, practical experiences and relevant soft skills associated with this course are to be taught and implemented, so that the student demonstrates the following industry oriented COs associated with the above mentioned competency:

a. Use number system and codes for interpreting working of digital system.
b. Use Boolean expressions to realize logic circuits.
c. Build simple combinational circuits.
d. Build simple sequential circuits.
e. Test data converters and PLDs in digital electronics systems.

4. TEACHING AND EXAMINATION SCHEME

Teaching Scheme			Credit (L+T+P)	Examination Scheme												
				Theory							Practical					
L	T	P		Paper Hrs.	ESE		PA		Total		ESE		PA		Total	
					Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min
4	-	2	6	3	70	28	30*	00	100	40	25#	10	25	10	50	20

(*): Under the theory PA, Out of 30 marks, 10 marks are for micro-project assessment to facilitate integration of COs and the remaining 20 marks is the average of 2 tests to be taken during the semester for the assessment of the cognitive domain UOs required for the attainment of the COs.

***Legends:** **L**-Lecture; **T** – Tutorial/Teacher Guided Theory Practice; **P** - Practical; **C** – Credit, **ESE** - End Semester Examination; **PA** - Progressive Assessment.*

5. COURSE MAP (with sample COs, PrOs, UOs, ADOs and topics)

This course map illustrates an overview of the flow and linkages of the topics at various levels of outcomes (details in subsequent sections) to be attained by the student by the end of the

course, in all domains of learning in terms of the industry/employer identified competency depicted at the centre of this map.

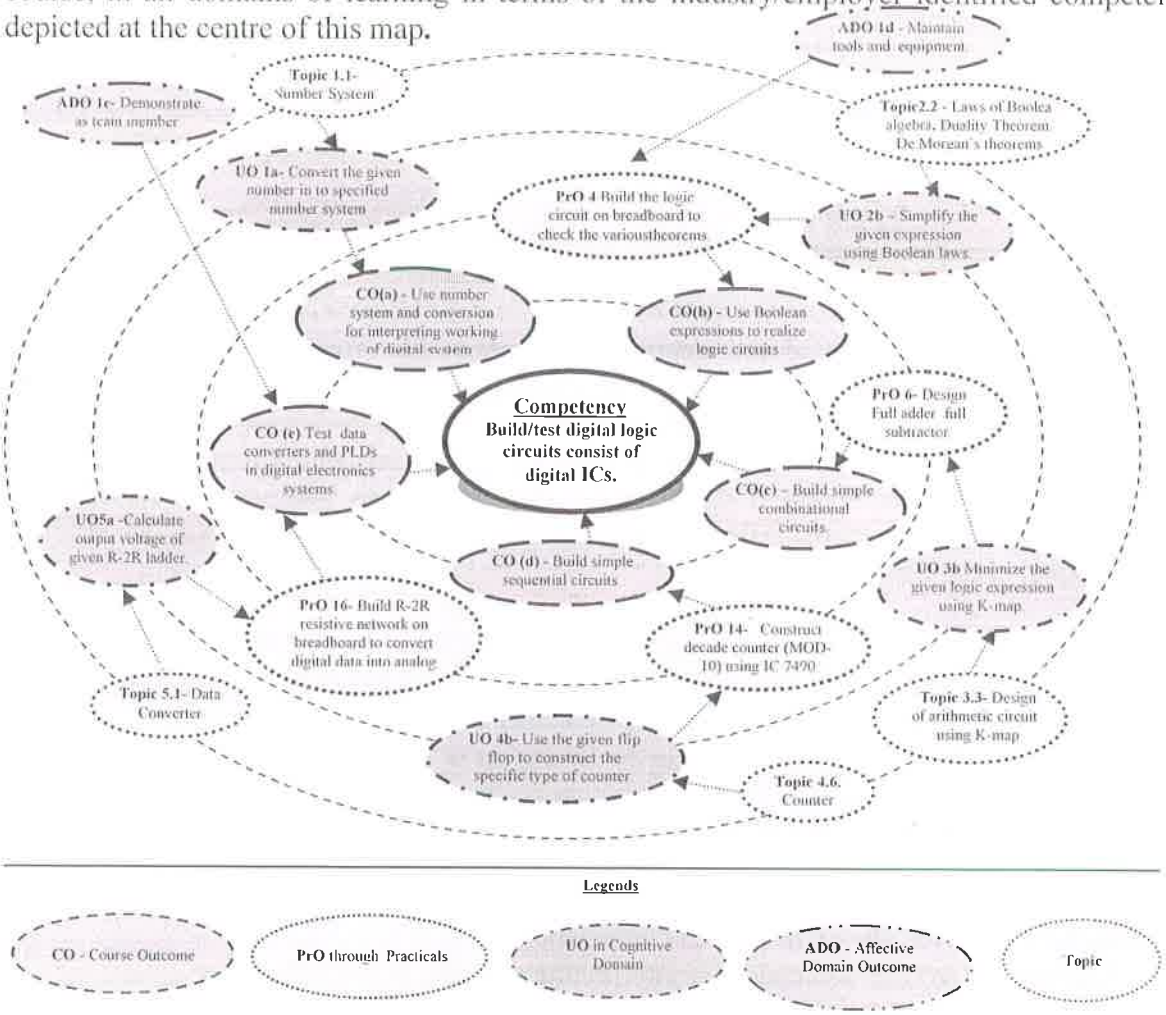

Figure 1 - Course Map

6. SUGGESTED PRACTICALS/ EXERCISES

The practicals in this section are PrOs (i.e. sub-components of the COs) to be developed and assessed in the student for the attainment of the competency.

S. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. required
1	Test the functionality of specified logic gates using breadboard. (IC 7404, 7408, 7432, 7486)	II	02*
2	Test the functionality of NAND and NOR gate of using breadboard (IC 7400 and 7402)	II	02
3	Construct AND, OR, NOT gates using universal gates.	II	02
4	Build the logic circuit on breadboard to check the De Morgan's theorems.	II	02
5	Design Half adder and Half subtractor using Boolean expressions.	III	02*
6	Design Full adder and full subtractor.	III	02
7	Construct and test BCD to 7 segment decoder using IC 7447/ 7448.	III	02
8	Build / test function of MUX 74151/74150/any other equivalant.	III	02

S. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. required
9	Build / test function of DEMUX 74155/74154/any other equivalant.	III	02
10	Build / test function of RS flip flop using NAND Gate.	IV	02*
11	Build / test function of MS JK flip flop using 7476.	IV	02
12	Use IC 7476 to construct and test the functionality of D and T flip flop.	IV	02
13	Implement 4 bit ripple counter using 7476.	IV	02
14	Use IC 7490 to construct decade counter (MOD-10).	IV	02
15	Implement 4 bit universal shift register.	IV	02
16	Build R-2R resistive network on breadboard to convert given digital data into analog.	V	02*
		Total	**32**

Note

i. *A suggestive list of **PrOs** is given in the above table. More such PrOs can be added to attain the COs and competency. A judicial mix of minimum 12 or more practical need to be performed, out of which, the practicals marked as '*' are compulsory, so that the student reaches the 'Precision Level' of Dave's 'Psychomotor Domain Taxonomy' as generally required by the industry.*

ii. *The 'Process' and 'Product' related skills associated with each PrO is to be assessed according to a suggested sample given below:*

S. No.	Performance Indicators	Weightage in %
a.	Preparation of experimental set up	20
b.	Setting and operation	20
c.	Safety measures	10
d.	Observations and Recording	10
e.	Interpretation of result and conclusion	20
f.	Answer to sample questions	10
g.	Submission of report in time	10
Total		**100**

The above PrOs also comprise of the following social skills/attitudes which are Affective Domain Outcomes (ADOs) that are best developed through the laboratory/field based experiences:

a. Follow safety practices.
b. Practice good housekeeping.
c. Demonstrate working as a leader/a team member.
d. Maintain tools and equipment.
e. Follow ethical practices.

The ADOs are not specific to any one PrO, but are embedded in many PrOs. Hence, the acquisition of the ADOs takes place gradually in the student when s/he undertakes a series of practical experiences over a period of time. Moreover, the level of achievement of the ADOs according to Krathwohl's 'Affective Domain Taxonomy' should gradually increase as planned below:

- 'Valuing Level' in 1st year

- 'Organising Level' in 2nd year
- 'Characterising Level' in 3rd year.

7. MAJOR EQUIPMENT/ INSTRUMENTS REQUIRED

The major equipment with broad specification mentioned here will usher in uniformity in conduct of experiments, as well as aid to procure equipment by authorities concerned.

S. No.	Equipment Name with Broad Specifications	PrO. S. No.
1	Digital Multimeter: 3 and ½ digit with R, V, I measurements, diode and BJT testing.	All
2	CRO : Dual Channel, 4 Trace CRT / TFT based Bandwidth 20 MHz/30 MHz X10 magnification 20 ns max sweep rate, Alternate triggering Component tester and with optional features such as Digital Read out.	16
3	Pulse Generator: TTL pulse generator	10-15
4	DIGITAL IC tester: Tests a wide range of Analog and Digital IC's such as 74 Series, 40/45 Series of CMOS IC's.	1-15
5	Bread Board Development System: Bread Board system with DC power output 5V, +/-12V and 0-5V variable , digital voltmeter , ammeter, LED indicators 8 no, logic input switches 8 no, 7 segment display 2 no, clock generator, Manual pulser, Breadboard with about 1,600 points, Potentiometer, relay etc	1-15
6	Trainer kits for digital ICs: Trainer kit shall consists of digital ICs for logic gates, flop-flop, shift registers, counter along with toggle switches for inputs and bi-colour LED at outputs, built in power supply.	1-15
7	Regulated power supply: Floating DC Supply Voltages Dual DC : 2 x 0 -30V; 0-2 A Automatic Overload (Current Protection) Constant Voltage and Constant Current Operation Digital Display for Voltage and Current Adjustable Current Limiter Excellent Line and Load Regulation	1-16
8	Trainer kit for 4 bit Counter using Flip Flops: 4 bit ripple counter, Synchronous Counter, IC 7476 based circuit. Input given by switches and output indicated on LED. Facility to select MOD 8 or MOD 16 mode. Built in DC power supply and manual pulser with indicator.	13

8. UNDERPINNING THEORY COMPONENTS

The following topics are to be taught and assessed in order to develop the sample UOs given below for achieving the COs to attain the identified competency. More UOs could be added.

Unit	Unit Outcomes (UOs) (in cognitive domain)	Topics and Sub-topics
Unit – I Number System and Codes	1a. Convert the given number into the specified number system. 1b. Perform the binary arithmetic operation on the given binary numbers. 1c. Convert the given coded number into the other specified code.	1.1 Number System: base or radix of number system, binary, octal, decimal and hexadecimal number system. 1.2 Binary Arithmetic: Addition, subtraction, multiplication, division. 1.3 Subtraction using 1's complement and 2's complement. Codes: BCD, Gray Code, Excess-3, and ASCII code.

Unit	Unit Outcomes (UOs) (in cognitive domain)	Topics and Sub-topics
	1d. Add the given two decimal numbers using BCD code.	1.5 BCD Arithmetic: BCD Addition
Unit – II Logic gates and logic families	2a. Develop the basic gates using the given NAND/NOR gate as universal gate. 2b. Simplify the given expression using Boolean laws. 2c. Develop logic circuits using the given Boolean expressions. 2d. Compare the salient characteristics of the given digital logic families.	2.1 **Logic gates**: Symbol, diode/ transistor switch circuit and logical expression , truth table of basic logic gates (AND, OR, NOT), Universal gates (NAND and NOR) and Special purpose gates (EX-OR, EX-NOR).Tristate logic 2.2 **Boolean algebra**: Laws of Boolean algebra, Duality Theorem, De-Morgan's theorems 2.3 **Logic Families**:Characteristics of logic families : Noise margin, Power dissipation, Figure of merit , Fan-in and fan-out, Speed of operation, Comparison of TTL, CMOS, types of TTL NAND gate
Unit– III Combinational Logic Circuits	3a. Develop logic circuits in standard SOP/ POS form for the given logical expression. 3b. Minimize the given logic expression using K-map. 3c. Use IC 7483 to design the given adder/ subtractor. 3d. Draw MUX/DEMUX tree for the given number of input and output lines. 3e. Write the specifications of the component for the given application. 3f. Develop the specified type of code converter.	3.1 **Standard Boolean representation:** Sum of Product (SOP) and Product of Sum(POS), Min-term and Max-term, conversion between SOP and POS forms, realization using NAND /NOR gates 3.2 **K-map reduction technique for the Boolean expression:** Minimization of Boolean functions up to 4 variables (SOP and POS form) 3.3 **Design of arithmetic circuits and code converter using K-map:** Half and full Adder, half and full Subtractor , gray to binary and binary to gray (up to 4 bits) 3.4 **Arithmetic circuits:** (IC 7483) Adder and Subtractor, BCD adder 3.5 **Encoder/Decoder:** Basics of encoder, decoder, comparison, (IC 7447) BCD to 7 segment decoder/driver 3.6 **Multiplexer and Demultiplexer:** working , truth table and applications of Multiplexers and Demultiplexures, MUX tree, IC 74151as MUX; DEMUX tree, DEMUX as decoder, IC 74155 as DEMUX 3.7 **Buffer:** Tristate logic, unidirectional and bidirectional buffer (IC 74LS244,74LS245)

Unit	Unit Outcomes (UOs) (in cognitive domain)	Topics and Sub-topics
Unit– IV Sequential Logic Circuit	4a. Use relevant triggering technique for the given digital circuit. 4b. Use the given flip-flop to construct the specific type of counter. 4c. Use excitation table of the given flip-flop to design synchronous counter. 4d. Design the specified modulo-N counter using IC7490. 4e. Construct ring/ twisted ring counter using the given flip-flop.	4.1 **Basic memory cell**: RS-latch using NAND and NOR 4.2 **Triggering Methods:** Edge trigger and level trigger 4.3 **SR Flip Flops**: SR-flip flop, clocked SR flip flop with preset and clear, drawbacks of SR flip flop 4.4 **JK Flip Flops**: Clocked JK Flip flop with preset and clear. race around condition in JK flip flop, Master slave JK flip flop, D and T type flip flop Excitation table of flip flops, Block schematic and function table of IC-7474, 7475 4.5 **Shift Register**: Logic diagram of 4-bit Shift registers – Serial Input Serial Output, Serial Input Parallel Output, Parallel Input Serial Output, Parallel Input Parallel Output, 4 Bit Universal Shift register **4.6 Counters:** Asynchronous counter: 4 bit Ripple counter, 4 bit up/down Counter, modulus of counter Synchronous counter: Design of 4 bit synchronous up/down counter Decade counter: Block schematic of IC 7490 Decade counter, IC 7490 as MOD-N Counter, Ring counter, Twisted ring counter
Unit– V Data Converters and PLDs	5a. Calculate the output voltage of the R-2R ladder for the given specified digital input. 5b. Calculate the output voltage of the weighted resistor DAC for the given specified digital input. 5c. Explain with sketches the working principle of the given type of ADC. 5d. Explain with sketches the working principle of the given types of memories. 5e. Explain with basic block diagram the working principle of the given type of programmable logic device.	5.1 **Data Converter**: DAC**:** Types, weighted resistor circuit and R-2R ladder circuit, DAC IC 0808 specifications ADC: Block Diagram, types, and working of Dual slope ADC, SAR ADC, ADC IC 0808/0809, specification 5.2 **Memory**: RAM and ROM basic building blocks. read and write operation ,types of semiconductor memories 5.3 **PLD:** Basic building blocks and types of PLDs, PLA, PAL, GAL 5.4 CPLD: Basic Building blocks, functionality.

***Note**: To attain the COs and competency, above listed UOs need to be undertaken to achieve the 'Application Level' and above of Bloom's 'Cognitive Domain Taxonomy'.*

9. SUGGESTED SPECIFICATION TABLE FOR QUESTION PAPER DESIGN

Unit No.	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Number System	06	2	2	4	08
II	Logic gates and logic families	10	4	4	4	12
III	Combinational Logic Circuits	16	4	6	8	18
IV	Sequential Logic Circuit	16	4	6	8	18
V	Data Converters and PLDs	16	4	4	6	14
Total		**64**	**18**	**22**	**30**	**70**

Legends: *R=Remember, U=Understand, A=Apply and above (Bloom's Revised taxonomy)*
Note*: This specification table provides general guidelines to assist student for their learning and to teachers to teach and assess students with respect to attainment of UOs. The actual distribution of marks at different taxonomy levels (of R, U and A) in the question paper may vary from above table.*

10. SUGGESTED STUDENT ACTIVITIES

Other than the classroom and laboratory learning, following are the suggested student-related ***co-curricular*** activities which can be undertaken to accelerate the attainment of the various outcomes in this course: Students should conduct following activities in group and prepare reports of about 5 pages for each activity, also collect/record physical evidences for their (student's) portfolio which will be useful for their placement interviews:

a. Prepare the survey report on the applications of different types of number system and code converters used in the design of digital system.
b. Compare technical specifications and applications of various types of memory, PLDs, CPLDs and Prepare report.
c. Test digital IC's using various testing equipment like digital IC tester, Digital multi-meter etc.
d. Give seminar on any course relevant topic.
e. Conduct library / internet survey regarding different data sheet and manuals.
f. Prepare power point presentation on digital circuits and their applications.
g. Undertake a market survey of different digital IC's required for different applications.
h. Search for video / animations / power point presentation on internet for complex topic related to the course and make a presentation.

11. SUGGESTED SPECIAL INSTRUCTIONAL STRATEGIES (if any)

These are sample strategies, which the teacher can use to accelerate the attainment of the various learning outcomes in this course:

a. Massive open online courses (***MOOCs***) may be used to teach various topics/sub topics.
b. ***'L' in item No. 4*** does not mean only the traditional lecture method, but different types of teaching methods and media that are to be employed to develop the outcomes.
c. About ***15-20% of the topics/sub-topics*** which is relatively simpler or descriptive in nature is to be given to the students for ***self-directed learning*** and assess the development of the COs through classroom presentations (see implementation guideline for details).
d. With respect to item No.10, teachers needs to ensure to create opportunities and provisions for ***co-curricular activities***.

e. Guide student(s) in undertaking micro-projects.
f. PPTs/Animations may be used to explain the construction and working of electronic circuits.
g. Guide students for using data sheets / manuals.

12. SUGGESTED MICRO-PROJECTS

Only one micro-project is planned to be undertaken by a student that needs to be assigned to him/her in the beginning of the semester. In the first four semesters, the micro-project are group-based. However, in the fifth and sixth semesters, it should be preferably be ***individually*** undertaken to build up the skill and confidence in every student to become problem solver so that s/he contributes to the projects of the industry. In special situations where groups have to be formed for micro-projects, the number of students in the group should ***not exceed three.***
The micro-project could be industry application based, internet-based, workshop-based, laboratory-based or field-based. Each micro-project should encompass two or more COs which are in fact, an integration of PrOs, UOs and ADOs. Each student will have to maintain dated work diary consisting of individual contribution in the project work and give a seminar presentation of it before submission. The total duration of the micro-project should not be less than ***16 (sixteen) student engagement hours*** during the course. The student ought to submit micro-project by the end of the semester to develop the industry oriented COs. Micro project report may be of four to five pages.

A suggestive list of micro-projects is given here. Similar micro-projects could be added by the concerned faculty:

a. Build a Digital IC tester circuit.
b. Build a 4bit parity generator and parity checker circuit.
c. Build a circuit to implement 4 bit adder.
d. Build a circuit to test 7 segment display.
e. Build a circuit to implement debounce switch.
f. Build a circuit for LED flasher.
g. Build a circuit for LED BAR display
h. Design and analyze digital arithmetic circuit

Note: *Use general purpose PCB for making micro projects*

13. SUGGESTED LEARNING RESOURCES

S. No.	Title of Book	Author	Publication
1	Modern Digital Electronics	Jain, R.P.	McGraw-Hill Publishing, New Delhi, 2009 ISBN: 9780070669116
2	Digital Circuits and Design	Salivahanan S.; Arivazhagan S.	Vikas Publishing House, New Delhi, 2013, ISBN: 9789325960411
3	Digital Electronics	Puri, V.K.	McGraw Hill , New Delhi, 2016, ISBN: 97800746331751
4	Digital Principles	Malvino, A.P.; Leach, D.P.; Saha G.	McGraw Hill Education, New Delhi, 2014, ISBN : 9789339203405
5	Digital Design	Mano, Morris; Ciletti, Michael D.	Pearson Education India, Delhi, 2007, ISBN: 9780131989245
6	Digital Electronics, Principles and Integrated Circuits	Maini, Anil K.	Wiley India, Delhi, 2007, ISBN: 9780470032145

S. No.	Title of Book	Author	Publication
7	Digital Fundamentals	Floyd, Thomas	Pearson Education India, Delhi, 2014, ISBN : 9780132737968

14. SUGGESTED SOFTWARE/LEARNING WEBSITES

a. www.cse.yorku.ca/~mack/1011/01.NumberSystems.ppt
b. www.people.sju.edu/~ggrevera/arch/slides/binary-arithmetic.ppt
c. www.mathsisfun.com/binary-number-system.html
d. www.codesandtutorials.com/hardware/electronics/digital_codes-types.php
e. www.ee.surrey.ac.uk/Projects/Labview/gatesfunc/
f. www.ee.surrey.ac.uk/Projects/Labview/boolalgebra/
g. www.eng.auburn.edu/~strouce/class/elec2200/elec2200-8.pdf
h. www.maxwell.ict.griffith.edu.au/yg/teaching/dns/dns_module3_p3.pdf
i. www.scs.ryerson.ca/~aabhari/cps213Chapter5.ppt
j. www.eng.wayne.edu/~singhweb/seql.ppt
k. www.cs.sjsu.edu/faculty/lee/Ch2Problems2.ppt
l. www.rogtronics.net/files/datasheets/dac/SedraSmith.pdf
m. www-old.me.gatech.edu/mechatronics_course/ADC_F04.ppt
n. www.allaboutcircuits.com/vol_4/chpt_13/3.html
o. www.youtube.com/watch?v=5Wz5f3n5sjs
p. www.eee.metu.edu.tr/~cb/e447/Chapter%209%20-%20v2.0.pdf
q. www2.cs.siu.edu/~hexmoor/classes/CS315-S09/Chapter9-ROM.ppt
r. www.cms.gcg11.org/attachments/article/95/Memory2.ppt
s. www.cosc.brocku.ca/Offerings/3P92/seminars/Flash.ppt
t. www.webopedia.com/TERM/R/RAM.html
u. www.cs.sjsu.edu/~lee/cs147/Rahman.ppt