# 17333 

## 16117

## 3 Hours / 100 Marks

Seat No.

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> Instructions: (1) All questions are compulsory.
> (2) Illustrate your answers with neat sketches wherever necessary.
> (3) Figures to the right indicate full marks.
> (4) Use of Non-programmable Electronic Pocket Calculator is permissible.

1. Attempt any six of the following :
a) i) Define w.r.t. digital IC's
1) Noise Immunity
2) Propagation delay.
ii) State advantages of digital systems (any 4).
iii) State any 4Boolean laws.
iv) Draw symbol and truth table of NoR gate.
v) Convert the following :
$(\mathrm{AB} 8 \mathrm{C})_{16}=(\quad)_{2}$
vi) Derive OR gate using NAND gates only.
vii) Draw the functional block diagram of ALU 74181.
viii) Define the following w.r.t. to DAC.
3) Resolution
4) Conversion time
b) Attemptany two of following.
i) Subtract using 2's complement method
5) $(10110)_{2}-(10001)_{2}$
6) $(1101)_{2}-(11010)_{2}$
ii) State and prove Demorgan's theorems.
iii) Convert the following :
7) $(498.25)_{16}=(\quad)_{10}$
8) $(10110101)_{2}=(\quad)_{16}$
9) $(\mathrm{B} 689 \mathrm{D})_{16}=(\quad)_{8}$
10) $(110110111)_{2}=(\quad)_{10}$
2. Attemptany four of the following :
a) Derive AMD gate and OR gate using NOR gates only.
b) Simplify the following Boolean expressions using Boolean laws:
i) $\overline{(A \bar{B}+\bar{A} \bar{B})(A B+\bar{A} B)}$
ii) $\bar{A} B+A B D+A \bar{B} C \bar{D}+B C$
c) Perform the following binary operations.
i) $101101 \times 110$
ii) $1101101 \div 1001$
d) Minimize the following Boolean expression using K-map.
$\mathrm{Y}=\Sigma \mathrm{m}(1,3,5,7,8,10,14)$
Draw the logical diagram using basic gates.
e) Design a half adder circuit using k-map.
f) Draw block diagram of digital comparator IC 7485 and explain with the help of truth table.
3. Attempt any four of the following:
a) Implement the logical expression using basic gates.

$$
\mathrm{Y}=\overline{\mathrm{A}} \mathrm{~B}+\overline{\mathrm{A}} \overline{\mathrm{~B}}+\overline{\mathrm{AC}}
$$

b) Design 1:16 demultiplexer using only 1:4 demultiplexers.
c) Convert the following expression into its standard forms.
i) $\mathrm{Y}=\overline{\mathrm{A}} \mathrm{BC}+\mathrm{AC}+\overline{\mathrm{B}}$
ii) $\mathrm{Y}=(\mathrm{B}+\overline{\mathrm{C}}) \bullet(\mathrm{A}+\mathrm{D}) \bullet(\overline{\mathrm{B}}+\overline{\mathrm{D}})$
d) Draw logic diagram of 8:1 multiplexer. Write it's truth table.
e) Explain different triggering methods.
f) Explain Master-Slave JK flip-flop with neat diagram.
4. Attemptany four of the following :
a) Draw the logical diagram of MOD -11 counter and describe its operation with truth table.
b) State any four specifications of ADC.
c) Describe the function of preset and clear terminals in JK flipflop. Write truth table of it.
d) Draw the neat diagram of clocked SR flip flop using NAND gates. Write truth table.
e) Differentiate between RAM and ROM - (any four points).
f) Draw the circuit diagram of weighted resister type D toA converter. Describe its working.
5. Attemptany four of the following :
a) Perform the following BCD arithmetic.
i) $(78)_{\mathrm{BCD}}+(59)_{\mathrm{BCD}}$
ii) $(86)_{\mathrm{BCD}}-(36)_{\mathrm{BCD}}$
b) Draw the logic diagram of D. flipflop using NAND gates. Write its truth table.
c) Reduce the following expression using k-map and implement it using NAND gates.

$$
\mathrm{Y}=\Pi \mathrm{M}(1,3,5,7,8,10,14)
$$

d) Design 4-bit asynchronous up counter and describe its operation.
e) Draw the block diagram of BCD to 7 -segment decoder. Write its truth table.
f) Draw the block diagram of SISO shift register and describe its operation.
6. Attemptany two of the following : ..... 16
a) i) State any two applications of counters. ..... 2
ii) Design full adder circuit using K-map. Implement using logic gates. ..... 6
b) i) Differentiate combinational and sequential logic circuits (2 pts). ..... 2
ii) State the applications of shift registers. ..... 2
iii) Draw the block diagram of 4-bit PIPO shift register and explain its working with timing diagram. ..... 4
c) i) Describe specifications of DAC. ..... 4
ii) Describe the working of successive approximation type $A$ to $D$ converter with neat diagram. ..... 4

