WINTER– 17 EXAMINATION

Subject Name: Principles of Digital Techniques  Model Answer

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more importance (Not applicable for subject English and Communication Skills.

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate’s answers and model answer.

6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate’s understanding.

7) For programming language papers, credit may be given to any other program based on equivalent concept.
1. a) Attempt any **six** of the following:  

(i) Draw symbol of EXOR gate and also write its truth table.

Ans:- (Symbol-1 mks, truth table- 1mks)

**Symbol**

![EXOR Gate Diagram](image)

**Truth table**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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<td>1</td>
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<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

(ii) Identify the functions of IC 0800 and IC 0809.

Ans:- (Functions-1 mks each)

1) 0800-8 bit ADC IC
2) 0809-8 Bit DAC IC

(iii) Convert the following binary number to gray code:

1) 1101001
2) 11111

Ans:- (Each conversion - 1mks each)
(iv) What is the role of Present and clear terminal of flip-flop?

Ans:- (Role of each terminal, 1 mkseach)

In the Flip-flop when the power is switched ON, the state of the circuit is uncertain. It may be set (Q=1) or reset (Q=0) state. In many applications it is desired to initially set or reset the flip-flop i.e. the initial state of flip-flop is to be assigned. This is done by using preset (Pr) & clear (Cr) inputs. There inputs may be applied at any time between clock pulses & are not in synchronism with the clock. Truth Table with Preset & Clear I/P.

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
<th>Operation performed</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>Cr</td>
<td>Pr</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>×</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>×</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

So, the O/P of the flip-flop changes whenever a clock signal is applied, it is necessary to set the output or reset the output i.e. to start with some definite initial state, then two additional inputs Preset & Clear are used. These inputs sets or resets the flip-flop independent of clock.
(v) Compare TTL and CMOS Logic families. (2 points)

Ans:- (Relevant 2 points of comparison- 1 mks for each point)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>CMOS</th>
<th>TTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device used</td>
<td>P-Channel &amp; N-Channel MOSFET</td>
<td>BJT (transistor)</td>
</tr>
<tr>
<td>Noise Margin</td>
<td>1.45 v</td>
<td>0.4v</td>
</tr>
<tr>
<td>Noise immunity</td>
<td>Better than TTL</td>
<td>Less than CMOS</td>
</tr>
<tr>
<td>Propagation delay</td>
<td>105 nsec</td>
<td>10 nsec</td>
</tr>
<tr>
<td>Switching speed</td>
<td>Less than TTL</td>
<td>Faster than CMOS</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>Less 0.1 mW</td>
<td>More 10 mW</td>
</tr>
<tr>
<td>Fan out</td>
<td>50</td>
<td>10</td>
</tr>
<tr>
<td>Unused input</td>
<td>Connect to ground or VCC</td>
<td>Input can remain floating &amp; treated as logic 1</td>
</tr>
<tr>
<td>Operating region</td>
<td>Ohmic &amp; cutoff region</td>
<td>Saturation or cutoff region</td>
</tr>
<tr>
<td>Component density</td>
<td>Need smaller space</td>
<td>Need more space than CMOS</td>
</tr>
</tbody>
</table>

(vi) What is Tristate buffer? Draw its symbol.

Ans:- (Definition- 1 mks, symbol-1 mks)

Tristate logic :- A tristate logic is a logical circuit that has three possible output states ie.

1) Logic 0
2) Logic 1 and
3) High impedance state

Symbol

![Tristate buffer symbol](image)
(vii) Define modulus of counter? How many flip flops are required for mod 5 counter?

Ans:-( Definition-1 mks, no. of flipflops required used -1 mks)

Modulus of a counter is defined as the no. of states or count through which the counter can progress. It depends on the no. of flipflops ‘N’ used. For ‘N’ no of flipflops used modulus or MOD is , MOD =2^N .

\[ N \leq 2^m \text{ where } N = \text{ no of states of counter} \]
\[ m = \text{ no of flip flops required.} \]
\[ 5 \leq 2^m \text{ .... for mod 5 counter; } N = 5 \]

Therefore, \( m = 3 \)

Ans: 3 flip flops are required for mod 5 counter.

(viii) State the necessity of multiplexer.

Ans:-( Need 2 points , 1 mks each)

- In most of the electronic systems, the digital data is available on more than one lines. It is necessary to route this data over a single line.
- Under such circumstances we require a circuit which select one of the many inputs at a time.
- This circuit is nothing else but a multiplexer which has many inputs, one output and some select inputs.
- Multiplexer improves the reliability of the digital system because it reduces the number of external wired connections.

b) Attempt any TWO of the following: Marks 8

(i) Convert the following into Binary and Add them \((A_{96})_{16} + (28_{16})_{16}\)

Ans:-(Correct answer – 4 mks)
(ii) Differentiate between Synchronous and Asynchronous counter.

Ans:- (4 points of differentiation- 4 mks)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Synchronous counter</th>
<th>Asynchronous counter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Definition</td>
<td>Clock pulses are applied simultaneously</td>
<td>Clock pulses are applied to first flipflop, output of first flipflop acts as clock pulses for next and so on.</td>
</tr>
<tr>
<td>Design Complexity</td>
<td>simple</td>
<td>complicated</td>
</tr>
<tr>
<td>Propagation Delay/speed</td>
<td>Less delay so more speed</td>
<td>More delay so less speed</td>
</tr>
<tr>
<td>Applications</td>
<td>High frequency applications</td>
<td>Low frequency applications</td>
</tr>
<tr>
<td>Problem of glitches</td>
<td>Absent</td>
<td>Present</td>
</tr>
</tbody>
</table>

Ans:- ( Circuit diagram using gates-2 mks, truth table- 2 mks)

![Circuit Diagram](image)

<table>
<thead>
<tr>
<th>E</th>
<th>S0</th>
<th>S1</th>
<th>Y0</th>
<th>Y1</th>
<th>Y2</th>
<th>Y3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
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<td>1</td>
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</tbody>
</table>

2. Attempt any Four of the following: Marks 16

a) Compare EPROM and flash memory.

Ans:- ( 4 points of comparison- 4 mks)
b) Describe operation of full adder with proper truth table and logical diagram.

Ans:– (Diagram- 2mks, truth table – 1mks, Theory/operation- 1mks)

A full adder is a combinational logic circuit that performs addition between three bits, the two input bits A and B, and carry C from the previous bit.

Block diagram

![Full Adder Block Diagram](image)

Truth Table

<table>
<thead>
<tr>
<th>Sr.No</th>
<th>Parameter</th>
<th>EPROM</th>
<th>Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Type</td>
<td>Non-volatile</td>
<td>Non-Volatile</td>
</tr>
<tr>
<td>2</td>
<td>Erasing Technique</td>
<td>Exposure to UV rays</td>
<td>Electrically</td>
</tr>
<tr>
<td>3</td>
<td>Time for erasing</td>
<td>Long 10 to 15 min</td>
<td>Instantly</td>
</tr>
<tr>
<td>4</td>
<td>Need to remove memory from the circuit</td>
<td>It is necessary to remove EPROM from the circuit for erasing.</td>
<td>Not necessary to remove from the circuit for erasing</td>
</tr>
<tr>
<td>5</td>
<td>Way of erasing</td>
<td>All the data gets erased</td>
<td>Selective erasing is possible.</td>
</tr>
<tr>
<td>6</td>
<td>Applications</td>
<td>In computer to store the operating system</td>
<td>Cell phones, digital camera etc.</td>
</tr>
<tr>
<td>Input</td>
<td>Output</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-------</td>
<td>--------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>B</td>
<td>Cin</td>
<td>Sum</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
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</tbody>
</table>

Circuit diagram using gates

Logic implementation of full adder:

![Full Adder Circuit Diagram]

c) Convert the following number into Binary:

(i) \((736.6)_8\)

(ii) \((2F9.25)_{16}\)

Ans:- (Each correct conversion – 2 mks)
d) State and prove De Morgan’s Theorems.

Ans:- (Each state and proof using table- 2 mks each)
i) $\overline{AB} = \overline{A} + \overline{B}$

It states that compliment of product is equal to sum of their compliments.

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>$\overline{AB}$</td>
<td>$\overline{A}$</td>
<td>$\overline{B}$</td>
<td>$\overline{A} + \overline{B}$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>0</td>
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</tr>
</tbody>
</table>

Column 03 = column 06
i.e. $\overline{AB} = \overline{A} + \overline{B}$
Hence proved

ii) $\overline{A+B} = \overline{A} \cdot \overline{B}$

It states that complement of sum is equal to product of their complements.

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>$\overline{A+B}$</td>
<td>$\overline{A}$</td>
<td>$\overline{B}$</td>
<td>$\overline{A} \cdot \overline{B}$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<td>0</td>
</tr>
</tbody>
</table>

Column 03 = column 06
$\therefore \overline{A+B} = \overline{A} \cdot \overline{B}$
Hence proved.

e) Draw the diagram of 3-bit twisted ring counter using JK F/F. Also write its truth table. Draw waveforms.

Ans:- (Diagram- 2 mks, truth table-1 mks, waveforms-1 mks)

Diagram
Truth table

<table>
<thead>
<tr>
<th>Clear</th>
<th>CLK</th>
<th>Q_2</th>
<th>Q_1</th>
<th>Q_0</th>
<th>Q_0 - Q_2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Initially</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>1</td>
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<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Waveforms
f) Draw the block diagram of successive approximation type ADC and explain its working.

Ans:- (Block diagram- 2 mks, working- 2 mks)
3. Attempt any Four of the following: 

Marks 16

a) Convert the following expression into their standard SOP form \( Y = A + BC + ABC + B \).

Ans:- (correct conversion- 4 mks)

\[
Y = A + BC + ABC + B \\
= A \cdot 1 + ABC + B \cdot (C \cdot 1 + B) \\
= A (C + B) (C + \bar{C}) + ABC + (A + \bar{A}) BC + B (A + \bar{A}) (C + \bar{C}) \\
= ABC + A \bar{B} C + \bar{A} B \bar{C} + \bar{A} B C + ABC + A \bar{B} C + \bar{A} B \bar{C} + \bar{A} B C \\
= ABC + A \bar{B} C + A B \bar{C} + A B C + ABC + A \bar{B} C + \bar{A} B \bar{C} + \bar{A} B C
\]
b) What is Race around condition and how it is eliminated?

Ans:- (Race around condition- 2 mks, methods to eliminate – 2 mks)

Race around condition occurs in J K Flipflop only when J=K=1 and clock/enable is high (logic 1) as shown below -

![Race around condition diagram](image)

Explanation:-In JK Flip-flop when J=K=1 and when clock goes high, output should toggle (change to opposite state), but due to multiple feedback output changes/toggles many times till the clock/enable is high. Thus toggling takes place more than once, called as racing or race around condition. Thus to avoid RAC following methods can be used-
1. Design the clock with time less than toggling time (this method is not economical)
2. Use edge triggering.

c) Solve the following using 1's and 2's complement method.

(i) \((42)_{10} - (63)_{10}\)

(ii) \((11010)_2 - (11100)_2\)

Ans:- ( Each conversion -1 mks )
(42)\_10 = (101010)\_2 = A

(63)\_10 = (111111)\_2 = B

(1) Using 1's comp. method

\[ 111111 - 000000 \]

2) Add to A

\[ \begin{array}{c}
101010 \\
+ 000000 \\
\hline
101010
\end{array} \]

3) As carry is not generated, result is negative, but in 1's comp. form -

So result is -

\[ 101010 \rightarrow (010101)\_2 \]

\[ = (-21)\_10 \]
(112)₁₀ = (101010)₂ = A
(6₃)₁₀ = (111111)₂ = B

8. Using 2's comp method
   a) Find 2's comp of B
      111111 \rightarrow 000000 + 1 \overline{000000} = 1000001

2) Add to A
   \[ \begin{array}{c}
   101010 \\
   + 000001 \\
   \hline
   101011
   \end{array} \]

2) As carry is not generated, result is negative, but in 2's comp form -20 the result is -
\[ \begin{array}{c}
101011 \rightarrow 010100 \\
+ 1 \\
\hline
010101
\end{array} \]

\( \text{ie } (-21)₁₀ \)
ii) \((11010)_2 \rightarrow (11100)_2\)

\[ A = (11010)_2 \]
\[ \beta = (11100)_2 \]

9) using 1's comp method

\[ \text{Find 1's comp of } \beta \]

\[ 11100 \rightarrow 00011 \]

2) add to A

\[
\begin{array}{c}
11010 \\
+ 00011 \\
\hline
11101 \\
\end{array}
\]

3) As carry is not generated

result is negative but

in 1's comp form 80

the result is -

\[ 1101 \rightarrow 00010 \]

\[(2)_{10}\]
b) using 2's comp method

1) find 2's comp of B

\[11100 \rightarrow 00011\]

\[+ 1\]

\[\frac{00100}{11110}\]

2) add to A

\[11010\]

\[+ 00100\]

\[\frac{11110}{11110}\]

3) As carry is not generated, result is negative, but in 2's comp form. So the result is -

\[11110 \rightarrow 00001\]

\[+ 1\]

\[\frac{00010}{00010}\]
d) What is priority encoder? Draw the truth and symbol table of decimal of BCD encoder.

Ans:- (Priority encoder definition- 1 mks, truth table -2 mks, symbol- 1 mks)

Encoder is a device which gives code corresponding to the active input. In priority encoder if two inputs active simultaneously output will be corresponding to the one which has higher priority.

E.g. IC 74147 Decimal to BCD priority encoder  OR  IC 74148 octal to binary priority encoder

![Fig: truth table of decimal to BCD encoder](image-url)

symbol
e) Draw 4 bit weighted resistor DAC and give expression for output voltage.

Ans:- (Diagram-2mks, expression- 2 mks)
Expression for output voltage:

\[ V_o = V_R \left[ d_1 \cdot 2^{-1} + d_2 \cdot 2^{-2} + \ldots + d_n \cdot 2^{-n} \right] \]

Where, \( V_0 \) = Analog output voltage

\( d_1, d_2 \ldots \ldots d_n \) are \( n \) bit digital input word with \( d_1 \) as MSB and \( d_n \) as LSB.

\( V_R \) = Reference voltage.

f) Reduce the following Boolean expression using Boolean laws.

i) \( Y = AB + AB + AB + A \bar{B} \)

ii) \( Y = ABC + ABC + ABC \)

Ans:- (Each reduction- 2 mks)

i)

\[ \bar{A}\bar{B} + \bar{A}B + AB + \bar{A}\bar{B} \]

\[ = \bar{A}\bar{B} + \bar{A}B + AB + \bar{A}\bar{B} \]

\[ = \bar{A}B + \bar{A}B + \bar{A}B + \bar{A}\bar{B} \]

\[ = \bar{A}(\bar{B} + B) + \bar{A}(B + \bar{B}) \]

\[ = \bar{A} + \bar{A} \]

\[ = 1 \]

\[ ; \bar{A} + \bar{A} = 1 \]
4. Attempt any Four of the following: Marks 16

a) Draw the internal diagram of IC 7490. Design mod 8 counter using IC 7490.

Ans:- (internal diagram of IC 7490- 2 mks, mod 8 counter using IC7490- 2 mks)

Internal diagram

Mod 8 counter
b) Explain with circuit diagram, the principle of TTL gate (NAND) with totem pole.

Ans:- (Diagram- 2 mks, truth table – 1 mks, explanation- 1 mks)
### Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

### Operating Principle:

1. **A and B both LOW (A = B = 0):**
   - If A and B both are connected to ground, then both the B-E junctions of transistors Q1 are forward biased.
   - Hence diodes D1 and D2 will conduct to force the voltage at point C to 0.7 V.
   - This voltage is insufficient to forward bias base emitter junction of Q2. Hence **Q2 will remain OFF**.
   - Therefore its collector voltage Vx rises to Vcc.
   - As transistor Q3 is operating in the emitter follower mode, output Y will be pulled up to high voltage.

Therefore, **Y = 1 (HIGH) ...**  
For **A = B = 0 (LOW)**
2. Either A or B LOW (A = 0, B = 1 or A = 1, B = 0):

• If any one input (A or B) is connected to ground with the other terminal left open or connected to +Vcc, the
  corresponding diode (D1 & D2) will conduct.

• This will pull down the voltage at “C” to 0.7 V.

• This voltage is insufficient to turn ON Q2. So it remains OFF.

• So collector voltage Vx of Q2 will be equal to Vcc. This voltage acts as base voltage for Q3.

• As Q3 acts as an emitter follower, output Y will be pulled to Vcc.

• Y = 1 ---- if A = 0 and B = 1
• ---- if A = 1 and B = 0

3. A and B both HIGH (A = B = 1):

• If A and B both are connected to +Vcc, then both the diodes D1 & D2 will be reverse biased and do not conduct.

• Therefore diode D3 is forward biased and base current is supplied to transistor Q2 via R1 and D3.

• As Q2 conducts, the voltage at X will drop down and Q3 will be OFF, whereas voltage at Z (across R3) will increase to turn ON Q4.

• As Q4 goes into saturation, the output voltage Y will be pulled down to a low voltage, Y = 0.

c) Calculate analog output of 4 bit DAC and digital input is 1011. Assume V_{fs} = 5V.

Ans:- (Formula – 1 mks, correct problem solving- 3 mks)
d) Compare sequential and combinational logic circuit. (Four points).

Ans:- ( Relevant four points of comparison – 4 mks)

<table>
<thead>
<tr>
<th>Sr no</th>
<th>Combinational ckt</th>
<th>Sequential ckt</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>The output at any instant of time depends upon the input present at that instant of time.</td>
<td>The output at any instance of time depends upon the present input as well as past input and output.</td>
</tr>
<tr>
<td>2</td>
<td>No memory element required in the circuit.</td>
<td>Memory element required to store bit</td>
</tr>
<tr>
<td>3</td>
<td>Clock not necessary</td>
<td>Clock is necessary</td>
</tr>
<tr>
<td>4</td>
<td>E.g. Adders, Subtractors, Code converters, comparators etc.</td>
<td>E.g. Flip flop, Shift registers, counters etc.</td>
</tr>
<tr>
<td>5</td>
<td>Used to simplify Boolean expressions, k-map, Truth table</td>
<td>Used in counters &amp; registers</td>
</tr>
</tbody>
</table>
e) Implement OR gate and AND gate using NAND gate.

Ans:- ( Each implementation – 2 mks)

\[ Y = \overline{A \cdot B} = A \cdot \overline{B} \]

\[ Y = \overline{A + B} = A \cdot \overline{B} \]

f) Compare single slope and dual slope ADC.

Ans:- ( Relevant 4points – 4 mks)
5. Attempt any Four of the following: Marks 16

a) Compare R-2R and binary weighted register.

Ans:- (Relevant 4points – 4 mks)

<table>
<thead>
<tr>
<th>Sr No.</th>
<th>Parameter</th>
<th>Weighted Resistor</th>
<th>R-2R Ladder Network</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Simplicity</td>
<td>Simple</td>
<td>Slightly complicated</td>
</tr>
<tr>
<td>2.</td>
<td>Range of resistor values</td>
<td>Wide range is required</td>
<td>Resistors of only two values are required</td>
</tr>
<tr>
<td>3.</td>
<td>Number of resistors per bit</td>
<td>One</td>
<td>Two</td>
</tr>
<tr>
<td>4.</td>
<td>Ease of expansion</td>
<td>Not easy to expand for more number of bits</td>
<td>Easy to expand</td>
</tr>
</tbody>
</table>

b) Define memory? Write down types of memory.
Ans:- (Definition- 1 mks, Types= 3 mks)

Memory- A sequential logic circuit and hence a group of flipflops that can store data in the binary form.

c) Draw PIPO shift register. State applications of shift register.

Ans:- (Diagram – 2 mks, applications-any 2 – 2 mks)

4 bit PIPO is as shown-

Applications – any 2

• There are so many applications of shift registers
  i. To produce time delay,
  ii. To simplify combinational logic
  iii. To convert the serial data to parallel data.
d) Design 16:1 MUX using 8:1 MUX.

Ans:- (Correct and relevant diagram - 4 mks)

![Diagram of 16:1 MUX using 8:1 MUX]

e) Give any four characteristics of CMOS and ECL logic families.

Ans:- (Relevant 4 characteristics of each - 1/2 mks)

CMOS-(any 4 characteristics)

- Lower static power dissipation
- Higher noise margins
- Higher packing density – lower manufacturing cost per device
- High yield with large integrated complex functions
High input impedance (low drive current)
Scaleable threshold voltage
High delay sensitivity to load (fan-out limitations)
Low output drive current (issue when driving large capacitive loads)
Low transconductance, where transconductance, $g_m \propto V_{in}$
Bi-directional capability (drain & source are interchangeable)
A near ideal switching device

ECL—any 4 characteristics

- Very fast switching with typical propagation delay of 360 ps—faster than TTL or CMOS.
- The standard ECL logic levels are nominally -0.8 V and 1.7 V for logical 1 and 0 respectively.
- Worst-case noise margins approximately 150 mV.
- ECL logic gates usually produce an output and its complement, eliminating the need for inverters.
- Current flow remains constant, eliminating noise spikes

f) Convert the following decimal numbers into excess-3 code

(i) $(5)_{10}$
(ii) $(25)_{10}$
(iii) $(46)_{10}$
(iv) $(144.4)_{10}$

Ans:-( Each correct conversion- 1 mks)
\[ (5)_{10} = (0101)_2 \]
\[
\begin{array}{c}
0 0 0 0 \\
0 1 0 1 \\
+ 0 0 1 1 \ (\text{add 3}) \\
\hline
1 0 0 0 \\
\end{array}
\]

\[ (25)_{10} = (0010 0101)_2 \]
\[
\begin{array}{c}
0 0 0 0 \\
0 0 1 0 0 1 0 1 \\
+ 0 0 1 1 0 0 1 1 \ (\text{add 33}) \\
\hline
0 1 0 1 1 0 0 0 \\
\end{array}
\]

\[ (46)_{10} = (0100 0110)_2 \]
\[
\begin{array}{c}
0 0 \\
0 1 0 0 + 1 1 0 \\
0 0 1 1 \ (\text{add 33}) \\
\hline
0 1 1 1 1 0 0 1 \\
\end{array}
\]
6. Attempt any Four of the following: Marks 16

a) Draw block diagram and explain working of dual slop ADC.

Ans:– (Block diagram– 2 mks, working – 2 mks)

The dual slope ADC consists of OPAMP’s being used as integrator and comparator. The control logic accepts the SOC signal and generates EOC signal when the conversion is over. It also controls the two switches S1 and S2 out of which S1 is a single pole three way switch whose one terminal is connected to analog voltage VA, second one is connected to ground and the third one is connected to a negative reference voltage -VREF.
Operation:- At the out Initially assume that the integrator output voltage $V_0=0$ and the counter is in RESET condition i.e. counter output is 00.

1. At $t = t_0$ switch S1 is connected to ground and switch S2 is closed. The capacitor CAZ gets connected across the comparator output.

2. Any offset voltage present in the OP-AMPS will appear across the capacitor C. This will provide an automatic compensation for the input offset voltage of all the amplifiers. Therefore integrator output voltage is zero for the interval $t_0$ to $t_1$.

3. At instant $t_1$ the SOC command is given to the control logic. Switch S1 is connected to VA and Switch S2 is open circuited. CAZ acts as a memory to hold the voltage required to keep the offset zero. Hence CAZ is known as the auto zero capacitor.

4. From $t_1$ to $t_2$, this ADC will integrate the analog input VA, for a fixed duration of clock cycles. This time interval is required for the counter to advance through all its possible output states, because for an n-bit counter there will be $2^n$ possible output states.

5. The counter output then reduces to zero. The time duration $t_1$ to $t_2$ is represented by $T_1$. The integrator output during this period is given by,

$$V_o = -\frac{1}{RC} \int_{t_1}^{t_2} V_A \, dt = \frac{-V_A T_1}{RC}$$

6. This expression represents a straight line with a slope of $-V_A / RC$. Thus we get a decreasing ramp. The time period $T$ is thus represented by $2^n$ clock cycles.

$$T = 2^n \times T$$

where $T$ = One clock cycle period

7. At the end of interval $T_1$ the integrator input is connected to a fixed negative reference voltage ($-V_{REF}$) via switch S1

8. The integrator output now starts increasing towards zero with positive slope. The slope of the line is $V_{REF} / RC$ for the duration $t_2$ to $t_3$. 

Page 35 of 41
9. The counter starts counting from 0. The integration will continue till the integrator output is non-zero. At instant $t_3$ the integrator output reduces to zero then the comparator output goes from HIGH to LOW and the clock pulses given to the counter are stopped.

10. At $t_3$, the counter output shows a number corresponding to $N$ clock cycles it has counted during period $t_2$ to $t_3$.

11. Thus this number $N$ represents the time taken for integrator output to reduce from $-VA$ to 0. Hence $N$ represents the desired digital output code proportional to the analog input $VA$.

12. If $VA$ increases, then the integrator capacitor will charge to a higher negative voltage during the time interval $T$. Therefore the time $T$ required to reduce the integrator output to zero increases.

13. Therefore the counter output count ($N$) will be higher. Thus $N$ is proportional to $VA$.

b) Describe working of SR latch using NAND gates with proper truth table.

Ans:- (Diagram- 2mks, working – 1 mks, truth table-1 mks)
c) Draw the block diagram of ALU IC 74181 and also write its operation.

Ans:- (Block diagram- 2 mks, operation- 2 mks)

Operation-

A 4 bit ALU does arithmetic and logical operations on 4 bits inputs A and B. Output is achieved on output F. The IC can perform 16 arithmetic and 16 logical operations that depend on mode control M.

For M=0, it does logical operation

For M=1, Arithmetic operation. The details of pins are as shown-
### Pin Descriptions

<table>
<thead>
<tr>
<th>Pin Names</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0–A3</td>
<td>Operand Inputs (Active LOW)</td>
</tr>
<tr>
<td>B0–B3</td>
<td>Operand Inputs (Active LOW)</td>
</tr>
<tr>
<td>S0–S3</td>
<td>Function Select Inputs</td>
</tr>
<tr>
<td>M</td>
<td>Mode Control Input</td>
</tr>
<tr>
<td>Cn</td>
<td>Carry Input</td>
</tr>
<tr>
<td>F0–F3</td>
<td>Function Outputs (Active LOW)</td>
</tr>
<tr>
<td>A = B</td>
<td>Comparator Output</td>
</tr>
<tr>
<td>G</td>
<td>Carry Generate Output (Active LOW)</td>
</tr>
<tr>
<td>P</td>
<td>Carry Propagate Output (Active LOW)</td>
</tr>
<tr>
<td>Cn+4</td>
<td>Carry Output</td>
</tr>
</tbody>
</table>

**d) Mention any eight Boolean laws.**

**Ans:** (Eight laws– ½ mks each)
e) Draw 3 bit synchronous counter with truth table and explain working.

Ans:- (Diagram- 2 mks, working – 1 mks, truth table – 1mks)
f) Draw and explain static RAM cell (TTL).

Ans:- (Diagram- 2 mks, explanation – 2 mks)
Static RAM cell with NMOS CELL

T2 & T4 are acting as resistances. X & Y lines are used for addressing cell. When X=Y=1 (high), the cell is selected. When X=1, the MOSFETS T5 & T6 are turned ON, which will connect memory cell to the data line and data bar line. When Y=1, the MOSFETS T7 & T8 are turned ON, which will make read & write operation possible.